Lab #9: NMOS and CMOS Inverter Circuits

Introduction

The *inverter*, or NOT gate, is the fundamental building block of most digital devices. The circuits used to implement the other Boolean functions (AND, OR, NAND, NOR, etc.) are typically derived from the basic inverter. Digital logic gates have been built using FETs, BJTs, and combinations of both kinds of transistors. A group of gates based on a given integrated circuit design approach comprises a *logic family*. Each logic family has its advantages and disadvantages, but CMOS is the dominant technology now. In this exercise you will compare the operation of a simple inverter based on a single *n*-channel MOSFET and a resistor to that of a CMOS inverter. The results will demonstrate partly why CMOS has achieved dominance in modern digital design.

Pre-Lab Work and Quiz

Read carefully the "Theoretical Background" and "Experimental Procedure" sections of this handout before the lab session. Think through the tasks you will be performing and try to visualize each test procedure. A two-question quiz will be administered at the beginning of the lab session.

Theoretical Background

The *i*-*v* characteristic of a typical *n*-channel MOSFET (also referred to as an NMOS device) is shown in Figure 1. The drain current i_D varies with the drain-to-source voltage v_{DS} at a level determined by the gate-to-source voltage v_{GS}. If $v_{DS} > v_{GS} - V_t$, where V_t is the threshold voltage of the MOSFET, then the drain current is essentially independent of v_{DS}. In that case, the

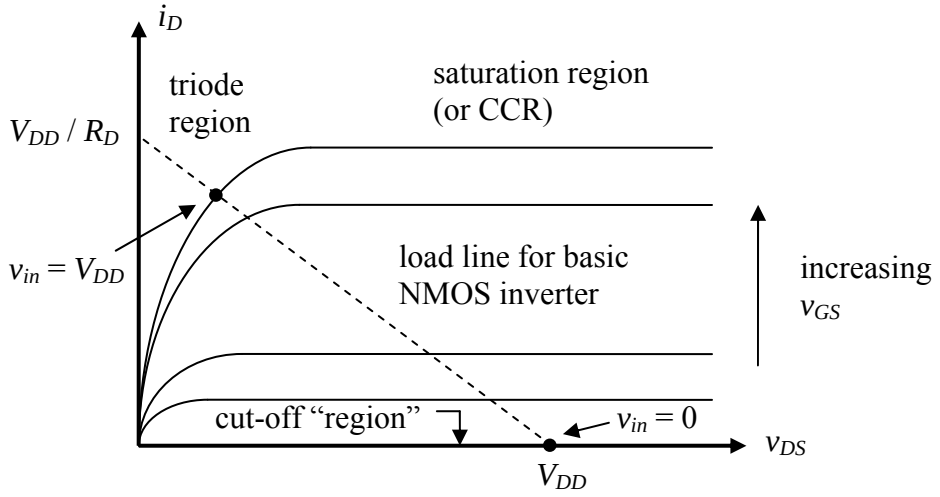

Figure 1. Typical *i*-*v* characteristic for an NMOS transistor. The set of *i*-*v* curves is overdrawn with a load line that represents the *i*-*v* characteristic of the power supply and resistor connected between the MOSFET's drain and ground.

MOSFET is said to operate in the *constant-current* or *saturation* region. If $v_{DS} < v_{GS} - V_t$, then the drain current varies with the drain-to-source voltage, and the MOSFET operates in the *triode* region. If $v_{GS} < V_t$, then no drain current flows, and the MOSFET is in *cut-off* mode.

In normal operation, voltage sources are not applied directly across the drain and source terminals of MOSFETs. Instead, combinations of resistors, voltage and/or current sources, and other circuit elements are connected to the device. The values of i_D and v_{DS} depend upon the characteristics of the external devices as well as the value of the gate-to-source voltage v_{GS}. For example, a simple inverter circuit based on an NMOS device is shown in Figure 2a. The values of i_D and v_{DS} in this circuit depend on the values of the resistor R_D and the power supply voltage V_{DD} in addition to v_{GS} (which is equal to v_{in} in this circuit).

In a typical digital circuit, logic level 0 is defined as ground potential (0 V), and logic level 1 is defined as the power supply voltage value (usually labeled V_{DD} in the case of circuits that employ FETs). Thus, the input voltage v_{in} in Figure 2a is either very close to 0 V or very close to V_{DD}. In practice, logic levels are usually assigned to ranges of voltages. For example, if the power supply voltage were +10 V, logic level 0 might correspond to the range 0-1 V while logic level 1 might correspond to 9-10 V. This allows for the small voltage drops that inevitably appear across various devices in the circuit or for sagging power supply voltages. In this example, voltages in the range 1-9 V are not allowed and would represent a circuit malfunction.

The values of i_D and v_{DS} that result from the application of a logical 0 or 1 to the input can be determined by drawing a load line over the *i*-*v* characteristic as shown in Figure 1. The load line represents the *i*-*v* characteristic of the voltage source V_{DD} and the resistor R_D, which is derived by applying KVL to the path from the power supply through R_D and the MOSFET's drain and source terminals to ground. That is,

$$V_{DD} = i_D R_D + v_{DS} \quad \rightarrow \quad i_D = -\frac{v_{DS}}{R_D} + \frac{V_{DD}}{R_D}.$$

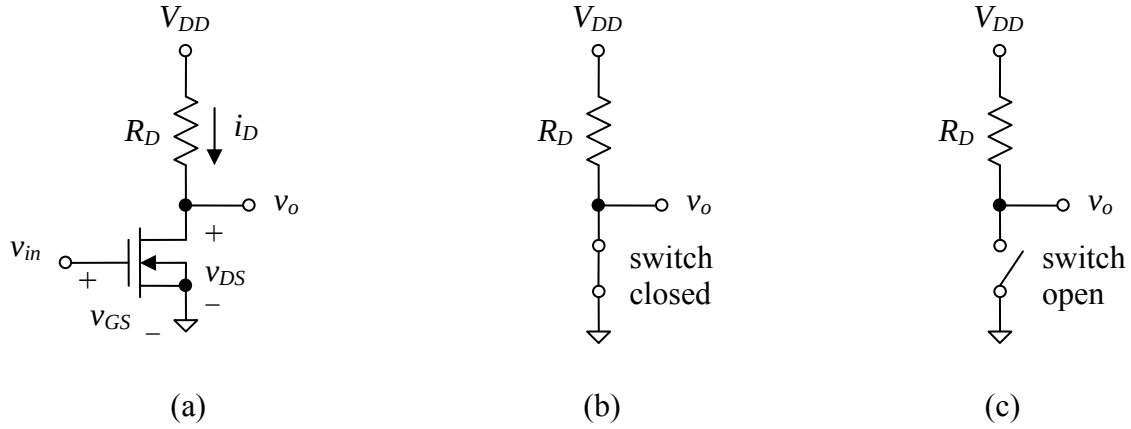

Figure 2. (a) Simple inverter based on a single NMOS device. (b) Approximate equivalent circuit for the case when the MOSFET is "on" (input is logical 1 and output is logical 0). (c) Equivalent circuit for the case when the MOSFET is "off" (input is logical 0 and output is logical 1).

The point where the two *i*-*v* characteristics intersect for a given value of v_{GS} (which equals v_{in} in this case) gives the values of i_D and v_{DS} for that value of v_{GS}. The use of a load line drawn over an *i*-*v* characteristic is the graphical equivalent of solving two equations (curves) in two unknowns (i_D and v_{DS}).

If v_{in} is close to V_{DD} (logic level 1), then $v_{GS} = V_{DD}$. The *i*-*v* characteristic for $v_{GS} = V_{DD}$ is represented by one of the upper curves in Figure 1. The load line intersects that curve at a point in the triode region near the vertical axis, which implies that v_{DS} is very small and that i_D is close to its maximum possible value (V_{DD}/R_D). Most of the power supply voltage (V_{DD}) is dropped across R_D. Since $v_o = v_{DS}$, and since v_{DS} is small, when the input is a logical 1 the output is a logical 0. An analogous representation of this situation is depicted in Figure 2b. The MOSFET is said to be "on" in this case, since it responds to a high input voltage by acting like an almost-short circuit between the drain and source.

If $v_{in} = 0$ (logic level 0), then $v_{GS} = 0$. The *i*-*v* characteristic for $v_{GS} = 0$ lies along the horizontal axis in Figure 1, which implies that the drain current i_D is zero regardless of v_{DS}. The load line intersects the $v_{GS} = 0$ curve at the horizontal axis, confirming that $i_D = 0$. In this case the MOSFET is said to be in the *cut-off* state. Since $i_D = 0$, there is no voltage drop across the drain resistor R_D, and the output voltage is equal to V_{DD}. An analogous representation of this situation is depicted in Figure 2c. In this case, the MOSFET acts as an open circuit and is said to be "off." Thus, when the input is a logical 0, the output is a logical 1. Note that it is assumed here that no current flows out of the output port; that is, it is assumed that the load resistance is infinite.

The circuit in Figure 2a is very simple, but it has a number of disadvantages. One of them is that the resistor occupies much more space on an integrated circuit chip than a FET. This is true in general of integrated resistors. The NMOS/resistor topology is therefore undesirable for large-scale integration. Another disadvantage will be explored later in the lab exercise.

The CMOS logic family does not use resistors at all. CMOS stands for *complementary* MOS, and it is characterized by logic gates made of both *n*-channel (NMOS) devices and *p*-channel (PMOS) devices. A CMOS inverter is shown in Figure 3. The lower transistor Q_n is the NMOS device, and Q_p is the PMOS device. Q_p is oriented so that its source is connected to V_{DD} and its drain to the drain of Q_n. The *i*-*v* characteristics of both FETs are shown in Figure 4. Note that the

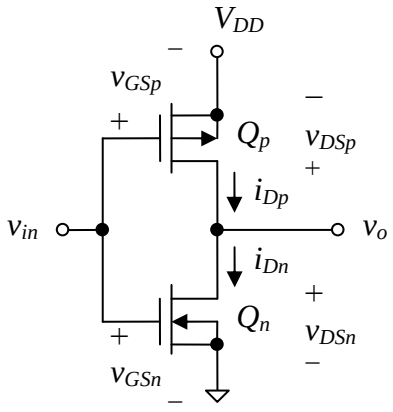

Figure 3. CMOS inverter circuit.

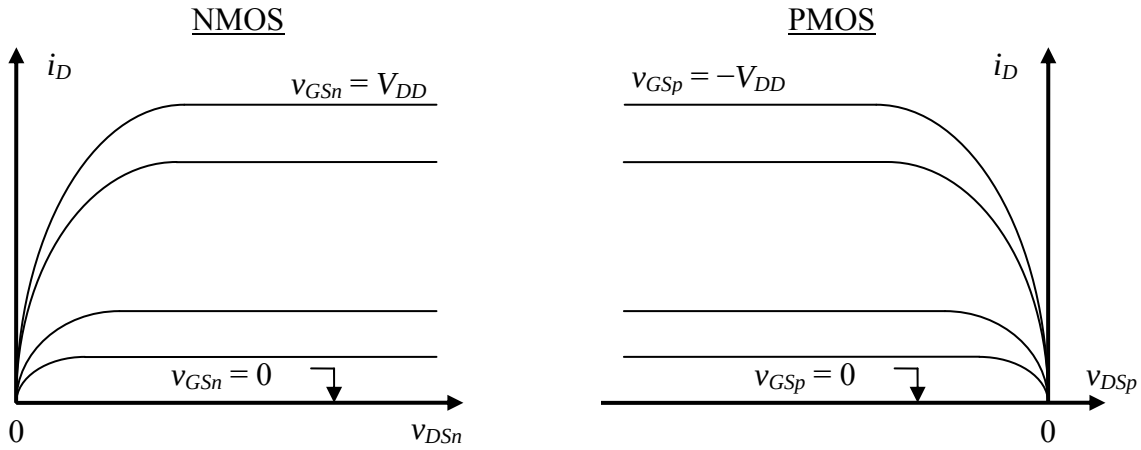

Figure 4. *i-v* characteristics for *n*-channel and *p*-channel MOSFETs.

drain-to-source voltage v_{DSp} of Q_p is negative. Furthermore, the value of v_{GSp} required for a non-zero drain current is negative. The threshold voltage V_{tp} is also negative for PMOS devices. The drain current i_{Dp} for the PMOS device is defined as flowing *out of* the drain, and the drain current i_{Dn} for the NMOS device flows *into* the drain. These definitions allow the drain currents to be expressed as positive values. In the case of the inverter, $i_{Dp} = i_{Dn}$.

When the CMOS inverter's input is a logical 0 (i.e., when $v_{in} = 0$), then $v_{GSn} = 0$ and $v_{GSp} = -V_{DD}$. This forces Q_n to turn off (almost an open circuit from drain to source) and Q_p to turn on (almost a short circuit). In this state, the output voltage v_o is very close to V_{DD}. When the input is a logical 1 ($v_{in} = V_{DD}$), then $v_{GSn} = V_{DD}$ and $v_{GSp} = 0$, which forces Q_n to turn on (short) and Q_p to turn off (open). In this second state, the output voltage v_o is close to zero. One of the major advantages of CMOS technology is that no resistors are required to construct any of the various logic gates. This allows a given gate to occupy much less space on a silicon wafer, which in turn allows more gates to fit on a chip of a given size. CMOS does have disadvantages, although many of them are shared with NMOS-only technology. One of them is that MOSFETs are highly susceptible to static discharges; however, once CMOS chips are in place on a circuit board they are usually safe. Another disadvantage is the relatively large capacitance between the gate and the substrate (equal to $C_{ox}WL$, where C_{ox} is the oxide capacitance per unit area W is the channel width, and L is the channel length). Its presence limits the maximum speed of CMOS circuits, since time must be allowed for the gate capacitance to charge or discharge after a logical state transition.

The CD4007 CMOS Chip

MOSFETs intended for use in small-signal applications (low currents and/or voltages) are not very common in discrete (individual transistor) form. Small MOSFETs are used primarily in digital logic ICs. One widely available digital IC is the CD4007 "dual complementary pair plus inverter." As shown in Figure 5, this chip consists of three *n*-channel and three *p*-channel MOSFETs in a single 14-pin DIP (dual inline package). The NMOS and PMOS devices have

matching *i-v* characteristics, since they are intended to be used in pairs in CMOS configurations. One NMOS device and one PMOS device are preconfigured as a CMOS inverter (pins 9-12); that is, their gates and drains are connected together internally as in Figure 3.

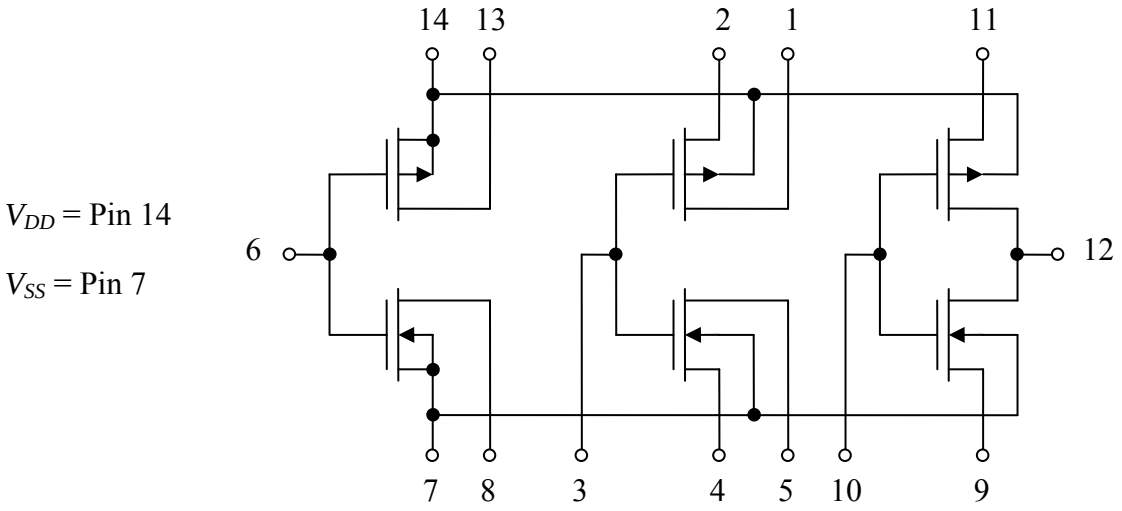

Figure 5. Pin-out for CD4007 dual complementary pair plus inverter.

The substrate for each PMOS device should be connected to the most positive point in the circuit (V_{DD}), and the substrate for each NMOS device should be connected to the most negative point (V_{SS}, which is usually 0 V). This avoids the possibility of forward-biasing the pn-junction between the substrate and one of the source terminals, a condition that could damage the device. Only one PMOS and one NMOS device in the CD4007 have their sources connected internally to the substrate (the left-most FETs in Figure 5). The sources of the other transistors must be connected to their respective substrates externally, if that is necessary. The PMOS substrates are all connected to pin 14, and the NMOS substrates are all connected to pin 7. **The safest mode of operation is to keep pin 14 connected to the positive side of the power supply and pin 7 connected to the negative side at all times, regardless of the circuit configuration. If any device's source becomes more negative (for NMOS) or more positive (for PMOS) than the substrate, that device could be destroyed.**

Experimental Procedure

Warning: Do not apply input signals to a CMOS circuit until power (V_{DD}) has been connected to it; otherwise, damage to the IC could result.

- Assemble the NMOS inverter shown in Figure 2a using the NMOS transistor connected to pins 6, 7, and 8 of the CD4007. The advantage of using this particular device is that its substrate is internally connected to the source, so you don't have to make the connection externally. Use a value of 47 kΩ for the drain resistor R_D, and use the 0-25 V power supply adjusted to +5 V for V_{DD}. Connect pin 14 (the PMOS substrate) to V_{DD} and pin 7 (the NMOS substrate) to ground.

- Connect the input of the inverter to Channel 1 of the oscilloscope and the output to Channel 2, and set the display to XY mode. You will have to figure out how to do this. The goal is to

create a display of the output voltage vs. the input voltage on the screen instead of a voltage vs. time. XY mode provides a visual depiction of the voltage transfer characteristic of the inverter. Set the resolution of both channels to 1 V/div, and make sure the BW limit function is activated on both channels. You might have to adjust the position controls once the circuit is activated to keep the transfer characteristic entirely on the screen. To improve the visual clarity of the display, move the origin of the plot to an intersection between major grid lines.

- Adjust the function generator so that it produces a triangle wave with a minimum voltage of 0 V and maximum of 5 V (i.e., an average value of 2.5 V). This will require you to set the DC offset to 2.5 V. Remember that the voltage displayed on the generator's readout assumes that a 50-Ω load is connected to the output, so interpret the readout carefully. The inverter's input impedance is very high. Set the frequency to 500 Hz or so. Once the function generator is properly adjusted, apply power to the inverter circuit, and connect the generator to the input of the inverter. What you should see is the voltage transfer characteristic of the inverter (i.e., v_o vs. v_{in}). Both the input voltage and the output voltage should range from 0 to 5 V.

- Show the displayed voltage transfer characteristic for your NMOS inverter to the instructor.

- Capture the screen image of the transfer characteristic displayed on the oscilloscope. Clearly mark the location of the origin and identify which grid lines correspond to the horizontal and vertical axes. Also, clearly indicate the parts of the curve that correspond to the cut-off region, the saturation region, and the triode region, and briefly explain how you separated one region from another.

- Now remove the function generator from the circuit, and connect the inverter's input terminal to the output of the 0-6 V power supply. **Keep the main power source (V_{DD}) on and connected to the circuit.** With the input voltage set to 0 V and then to 5 V, measure the drain-to-source voltage v_{DS} or the voltage across the drain resistor R_D. Using this data, calculate the total power dissipated by the circuit (drain resistor plus transistor) when the input is a logical 0 (0 V) and when it is a logical 1 (5 V).

- Remove **all** power from the circuit (both V_{DD} and v_{in}), and assemble the CMOS inverter shown in Figure 3. The wiring is a little less confusing if you use the on-chip inverter connected to pins 9-12. Remember to short pins 11 and 14 together and pins 7 and 9 together in order to connect the sources of the NMOS and PMOS devices to their respective substrates. Apply the power source (V_{DD}) to the circuit, and apply the same 0-5 V triangle wave used earlier to the input. Display the voltage transfer characteristic of the inverter on the oscilloscope using the XY display mode.

- Show the displayed voltage transfer characteristic for your CMOS inverter to the instructor.

- Capture the screen image of the transfer characteristic for the CMOS inverter, and compare it to that of the NMOS/resistor inverter. Pay particular attention to differences that might make one circuit superior to the other for use in digital logic applications. Explain the implications of the differences. You do not have to identify the regions of operation of the two transistors in the CMOS inverter.

- Remove the function generator from the circuit, and once again connect the 0-6 V power supply (adjusted to +5 V) to the input of the inverter. Measure the drain-to-source voltages v_{DSn} and v_{DSp} of both FETs using the bench-top voltmeter for a logical low input (0 V) and for a logical high input (5 V). The current that flows through the transistors is too small to measure using the laboratory instruments available to us. To obtain an estimate, consult the data sheet for the CD4007 and look for the appropriate "Quiescent Device Current" (or similar) rating. Using the voltage data you collected and the estimated current from the data sheet, calculate the approximate power dissipated by the circuit (the sum of that dissipated by both MOSFETs) for each input logic level.

- Compare the power dissipation of the CMOS inverter with that of the simple NMOS/resistor inverter for each state. Based upon your results, which circuit topology would you choose if you had to design a digital circuit under stringent power consumption limits? Explain why.

Adapted from:

Wasserman, M., *Laboratory Manual*, supplement to *Microelectronic Circuits and Devices*, 2nd ed., by M. N. Horenstein, Prentice-Hall, Inc., Upper Saddle River, NJ, 1996.

Grading

Each group must submit a brief but well written report that describes in detail all test configurations and the results of measurements. The report should include (but not necessarily be limited to) all of the details requested in the "Experimental Procedure" section. Items of particular importance include:

- Properly annotated screen capture of NMOS/resistor inverter voltage transfer characteristic
- Properly annotated screen capture of CMOS inverter voltage transfer characteristic
- Properly calculated power dissipation levels for each inverter circuit

The report is due at the beginning of next week's lab session. Each group member will receive the same grade, which will be determined as follows:

20% Quiz on pre-lab reading
30% Properly operating inverter circuits
30% Report – Completeness and technical accuracy
10% Report – Organization, neatness, and style (professionalism)
10% Report – Spelling, grammar, and punctuation