Lab #4: MOSFET Bias Design and Amplifier Analysis

Introduction

Biasing is the process of selecting component values in a transistor circuit so that the proper quiescent (DC average) voltages and currents are established to meet a set of design goals. It is a key step in the design of amplifier circuits and other types of circuits. A frequent requirement is to set and maintain the quiescent voltages and currents close to target values despite variations in device parameters. In other situations, the exact values of the voltages and currents are not so important, but their stability relative to temperature changes or other environmental variations *is* important. In this lab exercise, you will design, assemble, test, and compare two types of MOSFET bias circuits. You will then use the more stable circuit as the basis of an amplifier and observe and explain some of its performance characteristics. Group assignments are listed at the end of the handout. **Note that there is one required in-lab demonstration described in the middle of p. 3.**

Design Instructions and Specifications

- **Read and study** the lecture notes "Source Degeneration Biasing for Discrete MOSFET Amplifiers," which is available at the course Moodle site. It will be difficult to complete the design procedure below without the information summarized in the notes.

- Design a stabilized bias circuit like the one shown in Figure 1a for a 2N7000 or BS170 *n*-channel enhancement-mode MOSFET (i.e., find values for R_D, R_S, R_A, and R_B). Bias control is usually used in amplifier circuits. Thus, you may assume that the specifications below apply when the MOSFET operates in the saturation region. The design specifications are listed at the top of the next page.

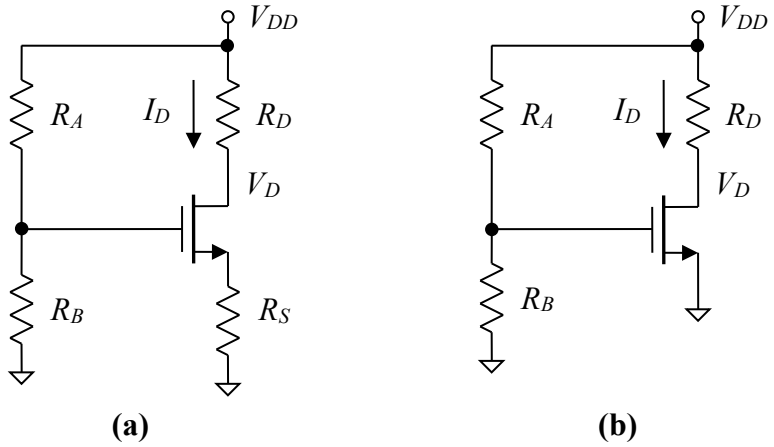


Figure 1. MOSFET biasing circuits that (a) uses a source degeneration resistor R_S or (b) fixes the value of the gate-to-source voltage.

Design specifications:

- Power supply voltage V_{DD}: 12 V
- Quiescent drain current I_D: 1.5 mA ± 0.2 mA
- Quiescent drain voltage V_D: 8.0 V ± 1 V
- Ensure that the current that flows through R_A and R_B is negligible compared to I_D, but do not use excessively large values for R_A and R_B; A single resistor with a value greater than 5–10 MΩ is too large.
- If possible, use only a single resistor for each of R_D, R_S, R_A, and R_B. Avoid combining resistors in series or parallel to match a calculated value more closely. All resistors must have values in the E24 series (standard values with 5% tolerance). Refer to the "Table of Standard Resistor Values" available at the ECEG 350 web site.

Carefully review the notes and additional requirements listed below:

1. Based on information available in the 2N7000 and BS170 MOSFET datasheets, reasonable estimates of the parameter values are $V_t = 2.1$ V and $k_n = 200$ mA/V^2. You may base your design on these nominal values; however, the actual values for your specific device could differ considerably from the estimated values. There is no way to know what the actual values are unless you measure them, but a design based on nominal values is a valid approach if the potential errors are bounded and sufficiently small. That is the case for this type of bias method.
2. The design problem is not fully constrained. Many combinations of resistor values will meet the specifications, so you will have to make some design choices. Consider factors such as the current drain on the power source, reliability, the input resistance of the circuit if used as part of an amplifier, etc.
3. Please notify me if the standard resistor values that you need are not available in the lab parts bins. Check the bins in the other Dana ECE labs if necessary.
4. Ensure that the power dissipation limits for the MOSFET and the resistors are not exceeded. You may combine resistors in series or parallel in place of a single resistor only if the predicted power dissipation is greater than 0.25 W.
5. If possible, select resistor values for each bias network using a deterministic process and not by trial and error. (This might not be possible for all of the resistors in the circuit in Figure 1b. In that case, limited use of trial-and-error is allowable.)
6. You may use Multisim or other circuit analysis software to check your design before you assemble the actual circuit. However, remember that the final design must be based on a deterministic process and not on trial-and-error. Also remember that the values for MOSFET parameters k_n, V_t, and λ in the software model most likely will not match those of the actual MOSFET that you use.
7. Keep careful records of your bias design process and test procedure since you will be asked to explain and justify them during your post-lab meeting.

Experimental Procedure

BEFORE YOU BEGIN: One in-lab demonstration is required. To ensure that you complete the lab exercise on time, you should strive to complete the demonstration either before the end of the first lab meeting or early in the second one. If the demonstration is not be completed during a lab session, there will be a 5-point score reduction.

- After you have completed your stable bias circuit design, assemble an actual circuit. Measure the quiescent drain voltage V_D, and determine the quiescent drain current I_D indirectly from your voltage measurements. Direct measurement of the current using the multimeter is too time-consuming. Confirm that both measured values are close to the specified values. You must determine whether the values are "close enough."

- Using a second MOSFET, design and assemble a separate fixed bias circuit (as in Figure 1b) to meet the same specifications as those for the stabilized bias circuit. The value of R_D must be found deterministically, but you should find that you have to use trial-and-error to find the values of R_A and R_B. Adjust their values until the drain voltage is within 10% or so of its specified value. You will almost certainly have to replace one or both resistors with a potentiometer to facilitate the adjustment. If you do, measure the resistance that the potentiometer adds to the circuit, and record the value.

- Perform a qualitative test of the stability of both bias circuits by warming each MOSFET using a hair dryer. Monitor the value of V_D, and continue applying heat until V_D stabilizes at a new value. Discuss the implications of the test with your group members and make sure that everyone understands what is happening. In particular, note whether the drain voltage rises or falls with temperature, and be able to explain the results in light of Figure 5 of the 2N7000 or BS170 datasheet. Also read Section 5.4.4 of the textbook (Sedra & Smith, 8th ed.) for further information. (The section is very short.) Think about how the temperature variation of V_t compares to that of k_n and the degree to which each quantity affects the value of I_D for the case when v_{GS} is barely greater than V_t and for the case when v_{GS} is much greater than V_t. That is, try to determine which parameter change dominates. **Demonstrate the thermal test to the instructor before moving on to the next item (This is the in-lab Demo, and it must be completed within a lab session)**.

- Now add a function generator, three capacitors, and a load to the stabilized bias circuit to form the common-source amplifier circuit shown in Figure 2 on the next page. Use the indicated component values and polarities. Pay attention to the guidelines listed below:

    - If any of the capacitors are electrolytic types, orient them as shown in the diagram (i.e., pay attention to where the positive ends connect).
    - Use a load resistance R_L of 100 kΩ.
    - The function generator is represented by the Thévenin equivalent circuit v_{sig} and R_{sig}. Its frequency should be set to 1.0 kHz and its amplitude to 5.0 mV pk (Thévenin equiv. voltage) if possible. Some function generators have a minimum setting of 20 mV pp, so a 20 dB attenuator might be needed to reduce the input voltage to the amplifier to a sufficiently low level. A 20 dB attenuator reduces an applied voltage by a factor of 0.1 (why?) while maintaining a specified Thévenin equivalent output resistance (in this case, 50 Ω).
    - **NOTE:** Alternatively, your group may assemble a common-gate amplifier with a 100-kΩ load and a function generator used as the signal source as above. **Groups that choose this option will earn 10 bonus points on their Lab #4 score** since it is a slightly more challenging design and rarely used in introductory electronics labs. Relevant circuit diagrams and background information will be provided.

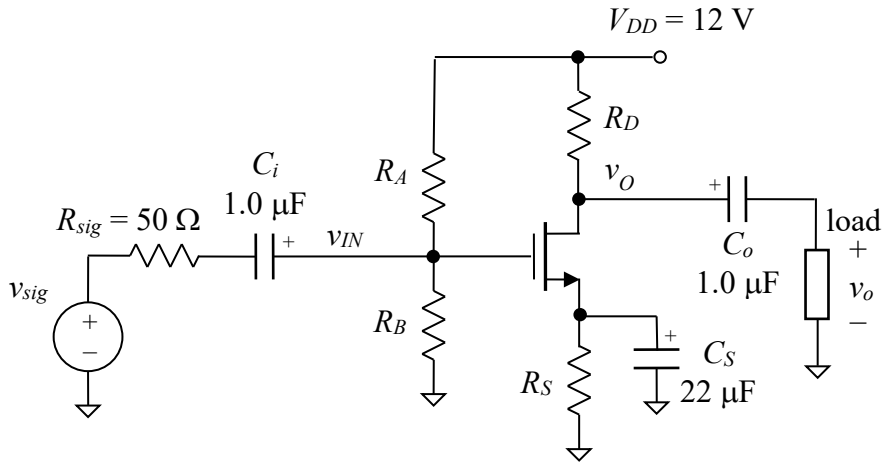


Figure 2. A basic common-source amplifier circuit.

- After the amplifier circuit has been assembled, apply power, and observe the input and output waveforms displayed on the oscilloscope. Adjust the oscilloscope's settings so that both waveforms are not too compressed in time and amplitude (i.e., so that the shapes of the two waveforms can be clearly seen). Make sure that neither the input nor the output waveform is experiencing distortion; they should be almost perfect sinusoids with no clipping and little to no flattening. The waveforms should be nearly symmetrical above and below the zero-volt level; if not, then some distortion is likely occurring, probably nonlinearity cause by the input voltage being too large. Use the distortion-free measured amplitudes to calculate the voltage gain v_o/v_{in} of the amplifier, where v_o and v_{in} are signal voltages, not total voltages. Record this value for the post-lab meeting.

  Remember that the value displayed on the function generator display could be half of the value of the actual Thévenin equivalent voltage v_{sig}. Measure to confirm!

- Using the measured bias voltages and/or currents that you obtained earlier and the known component values, calculate the value of the voltage gain via small-signal analysis (i.e., using the small-signal model of the MOSFET with g_m). Initially assume that V_t = 2.1 V and k_n = 200 mA/V^2 as you did for the bias design step above, but then repeat your calculations by assuming that k_n = 50, 100, and 300 mA/V^2 (with V_t = 2.1 V). Which set of assumptions yields the best agreement with your measured gain value? Save all four sets of calculations for discussion during the post-lab meeting.

- Finally, increase the amplitude of the input voltage while monitoring the output waveform. Make sure that the details of the output waveform's shape are easy to see. At some point, you should begin to observe noticeable distortion from the expected sinusoidal shape. Increase the input voltage amplitude enough to cause significant distortion of the positive and negative peaks of the output waveform. Be prepared to explain the most obvious distortion effects and their causes during your post-lab meeting. Make sure that you can properly associate the region of operation of the MOSFET with each waveform feature (i.e., positive clipping, negative clipping, and portions without distortion).

- Prepare for the post-lab meeting (length up to 25 min) that will take place during the Tuesday, Nov. 17 lab session. The following guidelines and instructions apply:

    - Read these guidelines and the "Post-Lab Meeting" section below well in advance of the meeting. You will need to prepare a set of visual aids.
    - **All tables must be formatted according to the guidelines posted at the course web site. Data tables must be prepared using software.**
    - **All equations, variables, and other mathematical content must be formatted according to the posted guidelines as well.**
    - All group members must be present, but you may leave after your meeting ends.
    - Meeting times will be determined randomly.
    - Meetings will not be rescheduled if the first one reveals circuit problems, wiring failures, errors in the test procedure, or a lack of preparation.
    - Deadline extensions will generally be approved for confirmed illnesses or other extenuating circumstances. Make-up meetings must take place before the end of Friday, Nov. 20 but not during a lecture, lab, or recitation section for another course or during important athletic, rehearsal, or similar commitments. Make-up meetings will use the Maker-E if neither Dana 305 nor Dana 307 is available.

  NOTE: Because of the compressed schedule during the lab sessions, one group from each session may request to meet later in the week. Requests must be made by 11:00 pm Sunday, Nov. 15. The first request received will be approved.

- Prepare a set of high-quality visual aids (neatly hand drawn is fine) to support your post-lab meeting. Include all relevant circuit diagrams with component values clearly labeled, all relevant equations, and anything else that might be helpful. **Tables must be prepared using software and formatted according to the guidelines posted on the Laboratory page at the web site. All equations, variables, and other mathematical content must be formatted according to the relevant guidelines as well.** All graphics must be well organized, neat, legible, and readily accessible to facilitate a lucid explanation. Leave out extraneous material. Include only items that improve clarity. Strive for completeness but avoid overwhelming amounts of visual clutter that detract from clarity. Imagine that you are explaining your work to an immediate supervisor (not a vice president or client).

  A good presentation must be technically accurate but must also have excellent oral and visual components that are well integrated. It must demonstrate that you have engaged deeply with the material and achieved a high level of understanding. It will be challenging to achieve a perfect score.

- Compile the visual aids that your group intends to use into a single PDF document (size less than 10 MB) and **e-mail** it to me before the post-lab meeting begins. If the PDF file is delivered after the meeting, each group member's Lab #4 score will be reduced by 5 points. Use a file name of the form

  LName1_LName2_LName3_Lab4_fa26.pdf,

  where "LName1," "LName2," and "LName3" are the group members' last names. Include the underscore (_) characters. Add "LName4" if your group has four members. Keep a copy to prepare for the next exam or if you need it for future reference.

Post-Lab Meeting

Each group must begin their meeting by demonstrating that the amplifier is operating properly. The output waveform must have a substantially larger amplitude than the input waveform and must not be significantly distorted if the input signal is at a sufficiently low level. Both waveforms must be clearly visible and easy to measure on the oscilloscope.

Each group member must then respond to one of the prompts from the numbered list below and possible follow-up questions. Each member's response will determine the individual portion of their score for Lab #4. The following guidelines and instructions apply:

- Each person will have a time limit of **seven minutes** in which to respond.
- You may assign the prompts to group members before the meeting.
- Organize the physical circuit layout and connections to equipment so that you can switch between demonstrations quickly.
- Excessive delays will affect group and/or individual scores as appropriate.

The four prompts are listed below. A two-person group must address Prompts #2 and #3:

1. [Not used in a 2-person group:] Explain the deterministic design process that your group followed for the four-resistor bias network. Justify any choices that were made to constrain the problem enough to obtain specific resistor values. Verify that the power limit specification of the MOSFET was not exceeded.
2. Explain how the voltage gain of the amplifier was determined using small-signal analysis. The explanation must be supported by a circuit diagram and a small-signal model, a derivation of the voltage gain expression, and a calculation of the parameter g_m. Compare the four calculated gain values to the measured gain value.
3. Explain the two most obvious impacts on the output waveform when the input amplitude is large enough to cause significant distortion. Explain why flattening of the positive and negative waveform peaks occurs and in what region (cut-off, saturation, or triode) the MOSFET operates in each case. Relate the observed distortion to the voltage transfer characteristic of the amplifier (Figure 7.4b in Sedra & Smith, 8th ed. for the CS amp).
4. [Four-person group only:] Demonstrate how the actual voltage gain of the amplifier was measured using the oscilloscope. Explain how the effects of distortion and noise were handled or minimized, whether peak or peak-to-peak measurements were used (and whether one or the other yielded better results and why), whether the function generator imposed any limitations.

Lab Scoring Criteria

Each group member will receive a score based on the following criteria quantized at the indicated point values. The first two criteria constitute a group base score; that is, each group member will receive the same score for those criteria. The remaining criteria will be assessed independently and will be determined by that person's contribution to the post-lab meeting. The rubrics posted on the Laboratory page at the course web site will guide the assessment of scores.

0, 8, 15, 23, 30 pts	Functional bias circuits with completion of in-lab demo (group)
0, 8, 15, 23, 30 pts	Functional amplifier circuit (group)
0, 8, 15, 23, 30 pts	Quality of response to prompt (indiv.)
0, 2, 5, 8, 10 pts	Quality and effectiveness of supporting visual aids (indiv.)

The following criteria can reduce or enhance lab scores for the group:

−5 pts	Biasing demo not completed during a lab session (group)
−5 pts	PDF of visual aids not delivered before post-lab meeting (group)
+10 pts	Common-gate amplifier is assembled (group)

If the meeting is completed after the deadline, a 10% score deduction will be applied for every 24 hours or portion thereof that it is late (not including weekend days or breaks) unless extenuating circumstance apply. No credit for the individual criteria will be given four or more days after the deadline; however, up to 60 pts will be assigned to each member of the group for the group criteria if at least one member demonstrates a functional circuit within one week of the deadline.

Group Assignments

The randomly generated groups for this lab exercise are listed below:

10:00 am Section:	Demo Completed	Amp Type
Behrens-Cruz Alvarez-Owusu-Ampiaw	___	CS CG
Hamdaoui-DeGraaff	___	CS CG
Johnston-Saint Jean-Saltsgiver	___	CS CG
Juca-Pappas-Waxman	___	CS CG
1:00 pm Section:		
Bell-Le (Declan)-MacGregor	___	CS CG
Le (Kevin)-Daniels-Le Quang	___	CS CG
Cowan-Francisco-Garfias-Ijomah	___	CS CG
Lorinkov-Offei-Koranteng-Perry-Yeo	___	CS CG

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