ECEG 350 **Electronics I** **Fall 2025**

Policies and Review Topics for Exam #3

The following policies will be in effect for the exam. They will be included in a list of instructions and policies on the first page of the exam:

1. You will be allowed to use a non-wireless enabled calculator, such as a TI-99.
2. You will be allowed to use three 8.5 × 11-inch two-sided handwritten help sheets. No photocopied material or copied and pasted text or images are allowed. If there is a table or image from the textbook or some other source that you feel would be helpful during the exam, please notify me.
3. All help sheets will be collected at the end of the exam but will be returned to you either immediately or soon after the exam.
4. Use of a help sheet that is not completely handwritten will result in an automatic 5-point score reduction.
5. If you begin the exam after the start time, you must complete it in the remaining allotted time. However, you may not take the exam if you arrive after the first student has completed it and left the room. The latter case is equivalent to missing the exam.
6. **You may not leave the exam room without prior permission except in an emergency or for an urgent medical condition. Please use the restroom before the exam.**

The exam will take place 8:00–9:50 am on Thursday, November 13 in Breakiron 066.

The following is a list of topics that could appear in one form or another on the exam. Not all of these topics will be covered, and it is possible that an exam problem could cover a detail not specifically listed here. However, this list has been made as comprehensive as possible. You should be familiar with the topics on the previous review sheets in addition to those listed below.

Although significant effort has been made to ensure that there are no errors in this review sheet, some might nevertheless appear. The textbook and the supplemental readings are the final authority in all factual matters, unless errors have been specifically identified there. You are ultimately responsible for obtaining accurate information when preparing for the exam.

Voltage regulation

- advantages over simple rectifier/filter design:
    - reduces output ripple voltage without using excessively large filter capacitor for a given load current
    - mitigates effects of variable power line (AC) voltage
    - mitigates effects of uncertainty (tolerance) of diode voltage drops, transformer secondary winding voltage, and internal resistances of transformer and diodes
- selection of bleeder resistor for filter capacitor in regulator circuits; capacitor discharges through voltage regulator as long as capacitor voltage is greater than $v_O + V_{DO}$ (or maybe a little less), but the bleeder resistor is necessary to complete the discharge
- zener diodes in reverse breakdown mode can be used as voltage regulators, but they are inferior to linear voltage regulators and switched-mode regulators (buck and boost converters)

Three-terminal voltage regulators (like the LM117 and LM317)

- selection of filter capacitors in regulator circuits
  - $V_{\max} = v_{\text{sec,pk}} - 2V_F$, where V_F = rectifier diode turn-on voltage
  - $V_{\min} = \left(\text{Buffer Factor}\right)\left(v_{O\max} + V_{DO}\right)$,
    where "Buffer Factor" = 1.4 to 1.8 (sets $V_{\min}$ value 40% to 80% higher than $v_{O\max} + V_{DO}$), $v_{O\max}$ = nominal output voltage, and V_{DO} = drop-out voltage of regulator
  - filter capacitor ripple for max. load current: $V_{rC} = V_{\max} - V_{\min}$
  - trade-off between capacitor value and transformer secondary voltage
  - time-average power dissipation of regulator and possible need for heat sink; can be approximated by $(v_{I\text{avg}} - v_O)i_{L\max}$
- input current (often labeled i_I) of three-terminal regulator is approximately equal to load current (often labeled i_L), especially at maximum rated load current
- regulators usually require a minimum output current (typically around 5–10 mA) to maintain specified output voltage
- relatively small capacitors (typically a few tenths of a μF to 1 μF) are sometimes mounted close to input and output terminals of regulator to maintain stability and suppress transient responses in practical circuits
- output voltage regulation can suffer if regulator device gets hot enough to activate internal protection circuitry
- output voltage regulation can also suffer if significant stray resistance is present between output terminal of regulator and load (stray resistance increases load regulation by an amount equal to the stray resistance)

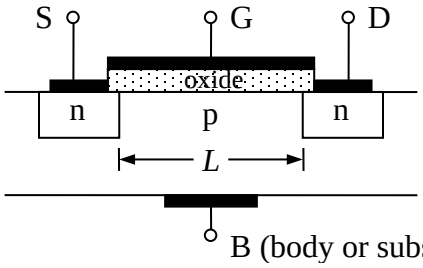
Load regulation

- definition: load regulation = $\dfrac{\Delta v_O}{\Delta i_L}$,
  where Δv_O is change in output voltage for given change in load current Δi_L for constant regulator input voltage v_I ("output" and "load" refer to the same thing)
- conversion of the % unit (used in datasheets) to the mV/mA unit and vice versa
- load regulation expressed in mV/mA is essentially the Thévenin equivalent (internal) resistance of the output port of the regulator
- load regulation is effectively increased by the resistance of the conductors (such as circuit board traces) between the regulator output terminals and the load; stray resistance of the output conductors degrades load regulation by increasing its value

Line regulation

- definition: line regulation = $\dfrac{\Delta v_O}{\Delta v_I}$,
  where Δv_O is change in output voltage for given change in line (input) voltage Δv_I for constant load current i_L (Δv_I is usually equal to the ripple on filter capacitor voltage)
- conversion of the %/V unit (used in datasheets) to the mV/V unit
- line regulation can be thought of as the ripple suppression or attenuation of the regulator; the ripple voltage on the filter capacitor on the input side is greatly reduced by the regulator so that the ripple voltage at the load on the output side is very small; i.e., the output ripple is a scaled down version of the input ripple
- When i_L increases, the capacitor and output ripple increase, and the time-average (and peak) output voltage drops.

"MOSFET" = Metal-Oxide Semiconductor Field Effect Transistor
Internal structure of enhancement-mode MOSFET (*n*-channel device shown below)



- gate is insulated from doped silicon by oxide or polymer layer
- device is usually symmetrical between source and drain (i.e., drain and source have same geometrical shape and size)
- channel lies inside substrate between source and drain regions and is usually only microns or a fraction of a micron in length (1 micron = 10^{-6} m)
- as of 2014, smallest channel length in commercially available FETs was 32 nm (p. 254 of Sedra & Smith, 7th ed.); 8th ed. lists a 28 nm process technology node
- L = channel length (inside distance from source to drain); W = channel width
- W/L = "aspect ratio"; usually, $W > L$

Qualitative understanding of operation of enhancement-mode MOSFET & fundamentals

- threshold voltage V_t
- effect of increasing v_{GS} (charge carriers flood region under gate insulation as v_{GS} rises above V_t, which forms channel); this is the reason for "enhancement" part of device name
- effect of increasing v_{DS} (channel bottom tilts as v_{DS} rises to a value comparable to v_{GS})
- directions and polarities of important currents and voltages (e.g., i_D and v_{DS})
- do not confuse drain current i_D in MOSFET with diode current i_D (context)
- depletion region around drain
- pinch-off condition occurs when FET is in saturation (constant-current) region; current still flows, but it does not continue to increase much with increasing v_{DS}
- electron and hole mobilities are dependent on process technology used (see Appendix K in Sedra & Smith, 8th ed.); typical values for doped silicon:
    - μ_n = 216 cm^2/V·s (for 65 nm process) to 550 cm^2/V·s (for 0.8 μm process)
    - μ_p = 40 cm^2/V·s (for 65 nm process) to 250 cm^2/V·s (for 0.8 μm process)
    - μ_n approx. 2–4 times μ_p
- μ_n (μ_p) and V_t are highly temperature dependent; both decrease with increasing temp.; μ_n (μ_p) usually dominates temperature behavior if v_{GS} is much larger than V_t
- capacitance of gate per unit area, $C_{ox} = \varepsilon_{ox}/t_{ox}$ (ε_{ox}, t_{ox} = permittivity and thickness of oxide layer); typical values are around 1–10 fF/μm^2
- process transconductance parameter $k'_n = \mu_n C_{ox}$ or $k'_p = \mu_p C_{ox}$; unit is A/V^2
- MOSFET transconductance parameter (includes aspect ratio W/L):

$$k_n = \mu_n C_{ox}\frac{W}{L} = k'_n\frac{W}{L} \quad \text{and} \quad k_p = \mu_p C_{ox}\frac{W}{L} = k'_p\frac{W}{L}$$

MOSFET *i-v* characteristic (i_D vs. v_{DS} for selected values of v_{GS}) & regions of operation

- cut-off region
    - $v_{GS} < V_t$
    - $i_D = 0$

- triode region
  - $v_{GS} > V_t$ and $v_{DS} < v_{GS} - V_t$
  - drain current expression for NMOS (similar for PMOS):

    $$i_D = k_n\left[\left(v_{GS} - V_t\right)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$
  - if $v_{DS} << v_{GS}$, MOSFET acts as voltage-controlled resistor (similar for PMOS):

    $$i_D \approx k_n\left(v_{GS} - V_t\right)v_{DS} \quad \rightarrow \quad \frac{v_{DS}}{i_D} = r_{DS} = \frac{1}{k_n\left(v_{GS} - V_t\right)}$$
  - drain-to-source resistance r_{DS} is relevant only when MOSFET acts as voltage-controlled resistor or as a switch in the on state (i.e., $v_{DS} << V_{GS} - V_t$); it is not applicable in the saturation region
- saturation region
  - $v_{GS} > V_t$ and $v_{DS} \geq v_{GS} - V_t$
  - simple drain current expression for NMOS (similar for PMOS):

    $$i_D = \frac{1}{2}k_n\left(v_{GS} - V_t\right)^2$$

    more accurate form that includes channel-length modulation:

    $$i_D = \frac{1}{2}k_n v_{OV}^2\left[1 + \lambda\left(v_{DS} - v_{OV}\right)\right] \approx \frac{1}{2}k_n v_{OV}^2\left(1 + \lambda v_{DS}\right)$$, where $v_{OV} = v_{GS} - V_t$

General analysis techniques for MOSFET circuits

- determination of region of operation (cutoff, saturation, or triode)
  - first determine whether $v_{GS} > V_t$ if possible
  - assume region of op., analyze circuit, then check assumption
  - if MOSFET is not cut off, it is usually easiest to assume saturation initially
- v_{DS} for *n*-channel MOSFETs is typically positive (negative for PMOS), although it can be close to zero for MOSFETs used in digital logic gates
- graphical analysis techniques (load lines) can be applied but are rarely used now
- resolution of sign ambiguities when quadratic formula is required due to square-law dependence of i_D on v_{GS} (or v_{DS} in triode region)

General amplifier concepts and background

- "analog" vs. "digital" electronics
- linear vs. nonlinear regions of operation
- concept of a signal; voltage and current signals
- concept of a circuit "port" (pair of terminals)
- concepts of signal sources and loads (TEC/NEC of a source includes a V or I source; TEC/NEC of a load contains no V or I source; both include equivalent resistance)
- distinguishing characteristics of "good" voltage amplifiers (very high input resistance and very low output resistance)

Distinctions between bias, signal, and total voltages and currents; basics of amplification

- signals are usually time-varying, but they do not have to be, or they might be quasi-static
- signals contain information (e.g., audio, video, encoded digital data, or sensor outputs proportional to physical quantities like temperature, pressure, or humidity, etc.)
- bias conditions (DC levels) define the "Q-point" (quiescent point or no-signal condition)
- total voltage or current is sum of bias and signal components (superposition)
- conventions:
  - lower-case variable w/upper-case subscript: total (bias + signal) quantity
  - upper-case variable w/upper-case subscript: bias (quiescent) quantity
  - lower-case variable w/lower-case subscript: signal (time-varying) quantity

Fundamentals of MOSFET amplifier circuits

- gate terminal insulated from substrate of MOSFET; bias and signal gate currents are zero
- voltage transfer characteristic (VTC)
  - plot of output voltage vs. input voltage
  - graphically expresses transfer function of MOSFET amplifier circuit
- most MOSFET amplifiers require the MOSFET to operate in the saturation region
- basic definition of small-signal voltage gain A_v (for NMOS devices; similar for PMOS; one of several ways to determine it):

$$A_v = \left.\frac{\partial v_O}{\partial v_{IN}}\right|_{v_{GS}=V_{GS}} \quad \text{or} \quad A_v = \left.\frac{\partial v_O}{\partial v_{IN}}\right|_{v_{IN}=V_{INQ}},$$

  where V_{GS} is the quiescent gate-to-source voltage and V_{INQ} is the quiescent input voltage
- for common-source (CS) inverter circuit with R_S bypassed by capacitor,

$$A_v = \frac{dv_O}{dv_{IN}} = \frac{dv_{DS}}{dv_{GS}} = \frac{d}{dv_{GS}}\left[V_{DD} - \frac{1}{2}k_n R_D \left(v_{GS} - V_t\right)^2\right] = -k_n R_D \left(v_{GS} - V_t\right)$$

  Note that gain is nonlinear (a function of v_{GS}) but is approximately linear if variation of v_{GS} is limited to a small range of values centered on the quiescent value V_{GS} such that $|v_{gs}| << 2(V_{GS} - V_t) = 2\ V_{OV}$; this is called the *small-signal condition*.
- Superposition can be applied to perform DC bias analysis and small-signal analysis separately; it greatly simplifies analysis in most cases.

DC blocking capacitors

- act as open circuits at DC (after transient phase when DC steady state applies)
- act as short circuits (or very low impedances or reactances) at signal frequencies
- isolate DC biasing from signal source and/or load
- impedance and reactance

$$Z_C = \frac{1}{j\omega C} = \frac{1}{j2\pi fC} = -j\frac{1}{2\pi fC} \quad \text{and} \quad X_C = -\frac{1}{\omega C} = -\frac{1}{2\pi fC} \quad \left(Z_C = jX_C\right)$$

AC bypass capacitors

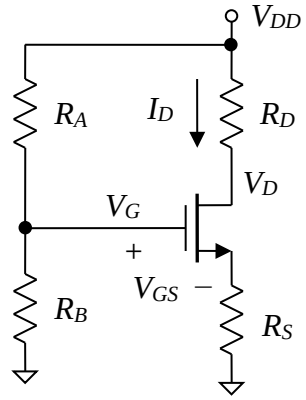
- act as open circuits at DC
- act as short circuits (or very low impedances or reactances) at signal frequencies
- ensure bypassed nodes are close to ground potential at signal frequencies
- commonly connected between power supply nodes and ground and across source (FETs) or emitter (BJTs) degeneration resistors

Biasing MOSFET circuits

- concept of biasing and why it is necessary
- parameters k_n, k_p, and $|V_t|$ usually exhibit wide variability from device to device due to loose manufacturing tolerances
- parameters k_n, k_p, and $|V_t|$ decrease with increasing temperature (strong dependence); $|V_t|$ change is approximately −2 mV/°C (−2 mV/K); minus sign indicates drop in value as temperature increases (i.e., a negative temperature coefficient or tempco)
- decrease in $|V_t|$ raises drain current, but decrease in k_n (or k_p) lowers drain current
- change in V_t usually dominates at low overvoltages ($V_{OV} = V_{GS} - V_t$), and change in k_n (or k_p) usually dominates at high overvoltages (e.g., Fig. 5 of 2N7000 datasheet)
- variation in k_n (k_p) is largely dominated by temperature dependence of μ_n (μ_p); $\mu_n \propto T^{-2.2}$
- design for quiescent output voltage, drain current, and/or voltage across source resistor
- MOSFET usually biased for operation in the saturation region if it is used as amplifier

- must pay attention to swing range of v_D (total voltage) to avoid cutoff and triode regions
  - saturation region defined by
    $v_{DS} \geq v_{GS} - V_t \quad \rightarrow \quad v_D - v_S \geq v_G - v_S - V_t \quad \rightarrow \quad v_D \geq v_G - V_t$
  - in cutoff region, $i_D = 0$; also true at boundary b/w cutoff and saturation regions
    - saturation-triode boundary defined by (for NMOS devices):
      $V_D\big|_{\text{sat.}-\text{triode}} = V_G - V_t$ or (equivalently) $V_{DS}\big|_{\text{sat.}-\text{triode}} = V_{GS} - V_t$

- "Four-resistor" bias network (source degeneration)



  - $I_D = 0.5k_n\left(V_{GS} - V_t\right)^2$ and $V_{GS} = V_G - I_D R_S$
  - square-law relationship → quadratic equations
  - must determine which of two solutions to quadratic equation is the physical solution
  - exact solution for drain current (NMOS):
    $$I_D = \frac{V_G - V_t}{R_S} + \frac{1}{k_n R_S^2} - \frac{1}{k_n R_S^2}\sqrt{1 + 2k_n R_S\left(V_G - V_t\right)}$$
  - design rules of thumb:

    $I_D R_D = I_D R_S = \frac{1}{3}V_{DD}$ (sometimes) and

    $V_G = I_D R_S + V_t + \sqrt{2I_D / k_n}$ (always);

    V_D value could be explicitly specified so that $I_D R_D \neq \frac{1}{3}V_{DD}$;

    value of $I_D R_S$ might be different as well to meet other constraints
  - V_{DS} (or V_D) sometimes made to exceed sat.-triode boundary by a specified amount
  - establishment of gate bias voltage simplified because $I_G = 0$: $V_G = V_{DD}\frac{R_B}{R_A + R_B}$,

    where R_B is the "lower" resistor (b/w gate and ground)

Relevant course material:

HW:	#5 and #6
Labs:	#3 and #4
Readings:	Assignments from Oct. 10 through Nov. 3, including the lecture notes: "Three-Terminal Linear Voltage Regulators" "Voltage Regulation and Power Conversion" "Source Degeneration Biasing for Discrete MOSFET Amplifiers"

This exam will focus primarily on the course outcomes listed below and related topics:

4. Analyze and/or design power supply circuits using linear voltage regulators.
5. Determine the region of operation of a MOSFET or BJT. [MOSFET only]
6. Determine and/or set the bias point (quiescent operating point) of a MOSFET or BJT circuit. [MOSFET only]

For all three outcomes, the focus will be only on circuits involving MOSFETs. There will be no problems involving PMOS (*p*-channel MOSFET) devices.
The course outcomes are listed on the Course Policies and Information sheet, which was distributed at the beginning of the semester and is available on the Syllabus and Policies page at the course web site. The outcomes are also listed on the Course Description page. Note, however, that some topics not directly related to the course outcomes could be covered on the exam as well.