ECEG 350 **Electronics I** **Fall 2024**

Homework Assignment #9 – due via Moodle at 11:59 pm on Monday, December 9, 2024

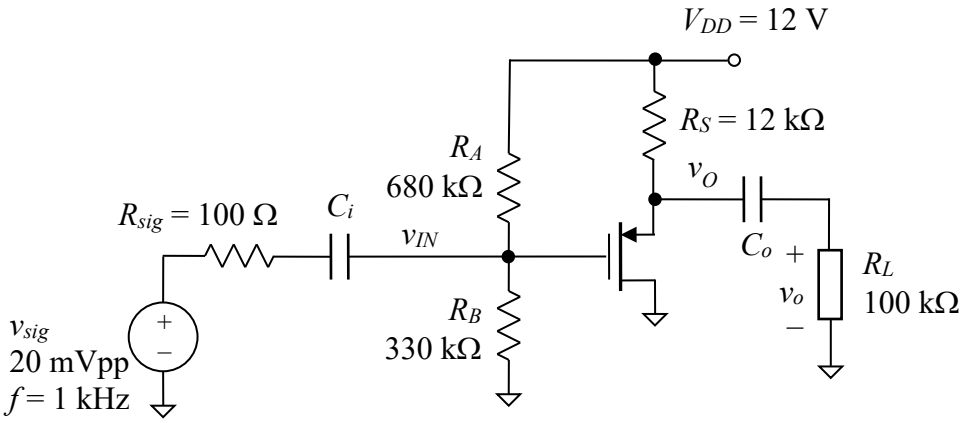
***Instructions, notes, and hints*:**

You may make reasonable assumptions and approximations to compensate for missing information, if any. Provide the details of all solutions, including important intermediate steps. You will not receive credit if you do not show your work.

The first few problems will be graded and the rest will not be graded. Only the graded problems must be submitted by the deadline above. Do not submit the ungraded problems.

***Graded Problems*:**

1. For the PMOS-based source follower circuit depicted below, find the numerical value of the quiescent drain current I_D. Also find the small-signal transconductance g_m. The MOSFET's parameters are $k_p = 100$ mA/V^2 and $V_{tp} = -2.0$ V. You may assume that $\lambda = 0$ (i.e., that channel-length modulation is negligible). *Note*: The formula for I_D that applies for NMOS devices with source degeneration will not work for this problem. You will have to modify the formula to work for PMOS devices or come up with another way to find I_D.



2. For the source follower considered in the previous problem, use an appropriate small-signal circuit model to find a symbolic expression for the voltage gain $A_v = v_o/v_{in}$, and then find the numerical value of the voltage gain with and without the MOSFET output resistance r_o included. All of the capacitors have negligible reactances at the signal frequency. The MOSFET has the parameters $k_p = 100$ mA/V^2, $V_{tp} = -2$ V, and $V_A = 40$ V ($\lambda = 0.025$ V^{-1}).

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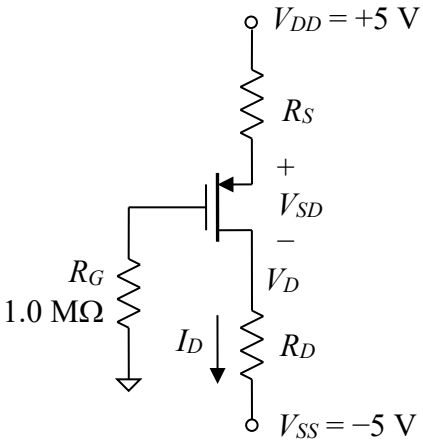
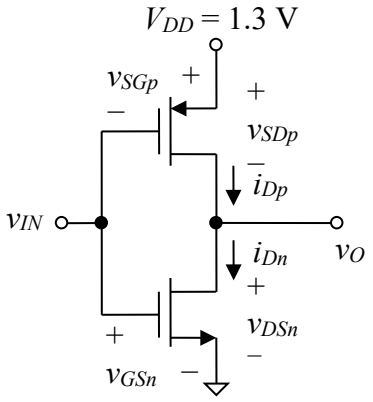
3. The circuit shown at right uses a bipolar power supply (±5 V) and a PMOS device with parameter values $V_t = -1.5$ V and $k_p = 30$ mA/V^2. The value of R_G has already been set. Find the values of R_S and R_D that result in a DC bias current of 2.5 mA and that cause the MOSFET to operate in the saturation region with a quiescent drain voltage that is 1.5 V away from the saturation-triode boundary. Ignore the channel-length modulation effect. *Note*: The positive power supply is labeled V_{DD} even though it is closest to the source terminal of the MOSFET. Likewise, the negative power supply V_{SS} is closest to the drain terminal. It is common for supply voltages to be labeled this way despite the apparent contradiction for PMOS devices; most engineers expect a voltage labeled V_{DD} to be positive and one labeled V_{SS} to be negative.
Hint: $V_{SD} > V_{SG} - |V_{tp}| \rightarrow V_D < V_G + |V_{tp}|$. (Why?)



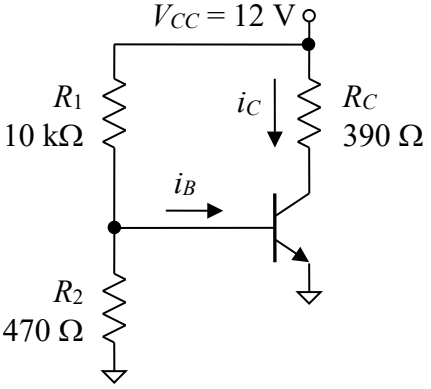
4. The MOSFETs in the CMOS inverter circuit depicted below are matched, which means that $V_{tn} = |V_{tp}|$ and $k'_n(W_n/L_n) = k'_p(W_p/L_p)$. Consequently, the circuit has the voltage transfer characteristic shown in Fig. 16.25 of Sedra & Smith, 8th ed. Suppose that the input transitions from logical 0 to logical 1 so that the input voltage v_{IN} increases from 0 V to V_{DD}. The load connected to the v_O terminal draws negligible current.

a. The drain currents (which are equal) have their maximum value when $v_{IN} = 0.5V_{DD}$, which causes both FETs to operate in the saturation region. Find the numerical value of the peak current for $V_{tn} = |V_{tp}| = 0.4$ V, $k'_n = 500$ μA/V^2, $(W_n/L_n) = 1.5$, and $V_{DD} = 1.3$ V. The values of k'_p and (W_p/L_p) are determined by the transistor matching condition; assume that $\mu_p = 0.25\mu_n$.

b. Find the upper limit V_{IL} of logic level 0 input voltages and the lower limit V_{IH} of logic level 1 input voltages. Also find the associated low-input noise margin NM_L and high-input noise margin NM_H. Compare them to the ideal value of $0.5V_{DD}$.



5. Explain why the silicon *npn* BJT in the diagram to the right operates in the cut-off region. Assume that the turn-on voltage V_F of the base-emitter junction is 0.7 V and that $V_{CE}|_{sat} = 0.2$ V. The β value of the BJT ranges from 100 to 300 depending on temperature and manufacturing variability.



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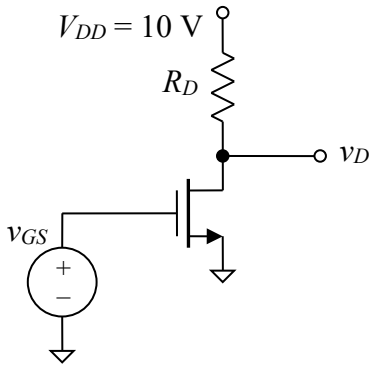
***Ungraded Problems*:**

The following problems will not be graded, but you should attempt to solve them on your own and then check the solutions. Do not give up too quickly if you struggle with one or more of them. Move on to a different problem and then come back to the difficult one after a few hours.

1. The test circuit shown below is used to measure the parameters k_n, V_t, and λ of an n-channel MOSFET. The data shown next to the figure were obtained as the drain resistor R_D was varied in value while v_{GS} was held at a value of 2.900 V using a precision power supply. Find the value of λ from the given data. You do not have to find the values of k_n and V_t, although you may do so if you wish. *Hint* #1: Equation (5.23) of the textbook (Sedra & Smith, 8th ed.) appears to be applicable here, but it is an approximation. A more accurate form is

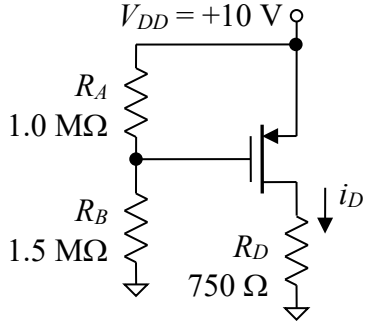
$$i_D = \frac{1}{2} k_n v_{OV}^2 \left[1 + \lambda\left(v_{DS} - v_{OV}\right)\right],$$

where $v_{OV} = v_{GS} - V_t$ (v_{OV} is the "overvoltage"). The channel-length modulation parameter λ is equal to the reciprocal of the Early voltage V_A. Figure 5.17 in the textbook should help you see the significance of this fact as it applies to solving this problem.

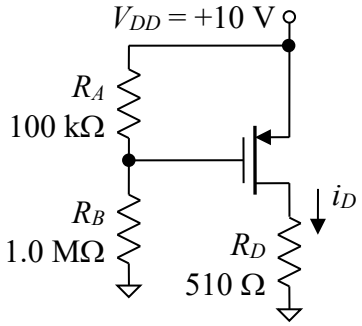


R_D (Ω)	v_D (V)
75	7.256
100	6.402
150	4.776
220	2.668
270	1.270

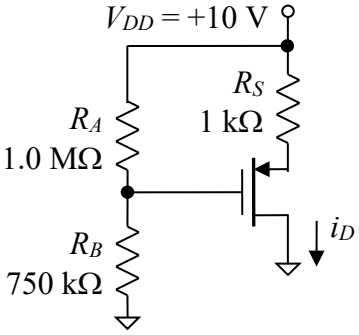
2. Find the regions of operation of the PMOS devices in the circuits shown below, and find the drain current i_D and source-to-drain voltage v_{SD} for each case. The MOSFETs' parameters are $k_p = 10$ mA/V^2 and $V_{tp} = -2.0$ V. You may assume that $\lambda = 0$ (i.e., there is no channel-length modulation).



(a)



(b)



(c)

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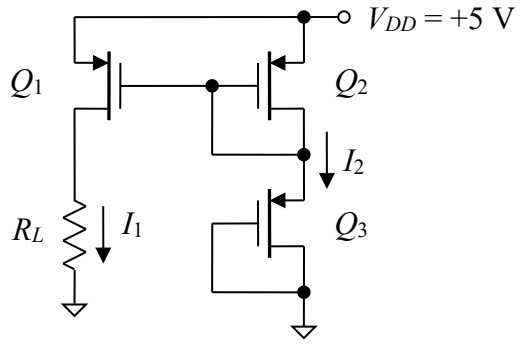
3. The circuit shown below is called a *current mirror* because it is designed to cause the current I_1 flowing through the load represented by resistance R_L to be the same as current I_2, the value of which is determined by adjusting the dimensions of Q_2 and Q_3. In effect, the circuit acts like an almost ideal current source for the load. (The channel-length modulation effect and other practical limitations keep it from being ideal, but you may ignore channel-length modulation here.) All three PMOS devices are fabricated on the same silicon die with $\mu_p C_{ox}$ = 58 μA/V^2, L = 800 nm, and $V_t \approx -0.7$ V. Transistors Q_1 and Q_2 both have channel widths of 2.16 μm. You may assume that $\lambda = 0$ and that Q_1, Q_2, and Q_3 are all operating in the saturation region, which is a necessary condition for the circuit to operate properly. Current mirrors are often used to establish controlled bias currents in integrated circuit amplifiers.

- **a.** Find the required channel width of Q_3 so that the load current I_1 is equal to 50 μA. Show why $I_1 = I_2$ (a very simple proof).
- **b.** Because Q_2 and Q_3 are in the so-called diode-connected configuration (so that $v_{SD} = v_{SG}$), they always operate in the saturation region if they are not cut off. Find the range of values of R_L for which Q_1 also operates in the saturation region.
- **c.** Explain how the width W_1 of Q_1 could be altered, and by how much, so that $I_1 = 3I_2$. The widths of Q_2 and Q_3 would remain unchanged.



4. Equations (16.37) and (16.38) in the textbook (Sedra & Smith, 8th ed.) give the high-input and low-input noise margins for a CMOS inverter in which the MOSFETs are matched in the sense that $V_{tn} = |V_{tp}|$ and $k'_n(W_n/L_n) = k'_p(W_p/L_p)$. Recall from Sec. 16.2.3 of the textbook that an ideal inverter would have $NM_L = NM_H = 0.5V_{DD}$. Find the common value of the threshold voltage magnitude V_t that both the NMOS device and the PMOS device must have to achieve ideal noise margins. Note: Given that the value of V_t cannot be set with high precision using current fabrication methods, the value of V_t in practical inverter circuits is substantially lower than the "ideal" value that would yield $NM_L = NM_H = 0.5V_{DD}$. As explained in Chap. 17 of the textbook, high V_t values, especially those approaching the "ideal" value, lead to greatly reduced switching speeds between logical states.