ECEG 350 **Electronics I** **Fall 2024**

Homework Assignment #8 – due via Moodle at 11:59 pm on Friday, Nov. 15, 2024

***Instructions, notes, and hints*:**

You may make reasonable assumptions and approximations to compensate for missing information, if any. Provide the details of all solutions, including important intermediate steps. You will not receive credit if you do not show your work.

The first few problems will be graded and the rest will not be graded. Only the graded problems must be submitted by the deadline above. Do not submit the ungraded problems.

***Graded Problems*:**

1. Shown on the next page is a common-source (CS) amplifier that uses four-resistor biasing. The load has an equivalent resistance of 2.5 MΩ, so it can be ignored for gain calculations. The circuit uses the biasing rule-of-thumb $I_D R_D = I_D R_S = V_{DS} = V_{DD}/3$. The quiescent drain current is around 1.0 mA, and the voltage gain is $A_v = v_o/v_{in} = -40$ V/V. The magnitude of the input voltage v_{in} must be less than 40 mV to satisfy the small-signal condition (a factor of 1/10 corresponds to "much less than").

Higher gain can be achieved by distributing the quiescent voltages differently. Since $R_L >> R_D$, then

$$A_v \approx -g_m R_D = -\sqrt{2k_n I_D}\,R_D = -\sqrt{2k_n I_D}\left(\frac{I_D R_D}{I_D}\right) = -\sqrt{\frac{2k_n}{I_D}}\left(I_D R_D\right),$$

which suggests that the gain of a CS amplifier can be increased by increasing the quiescent voltage across R_D (i.e., the voltage $I_D R_D$) and/or decreasing the quiescent drain current. However, increasing the voltage $I_D R_D$ can push the quiescent point closer to the triode region unless the voltage across R_S (the voltage $I_D R_S$) is reduced as well because, by KVL,

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S \quad \rightarrow \quad V_{DS} = V_{DD} - I_D R_D - I_D R_S,$$

but we need to maintain $V_{DS} > V_{GS} - V_t$.

The *total* voltage v_{DS} fluctuates if a signal is present, so the *bias* value V_{DS} must be comfortably above V_{OV}. Reducing the voltage across R_S results in less stable bias conditions, so this approach represents a trade-off. If the value of I_D is reduced to increase the gain, then the small signal condition becomes more constrained because

$$I_D = \frac{1}{2}k_n\left(V_{GS} - V_t\right)^2 = \frac{1}{2}k_n V_{OV}^2 \quad \rightarrow \quad V_{OV} = \sqrt{\frac{2I_D}{k_n}} \quad \text{and} \quad \left|v_{gs}\right| << 2\left(V_{GS} - V_t\right) = 2V_{OV}.$$

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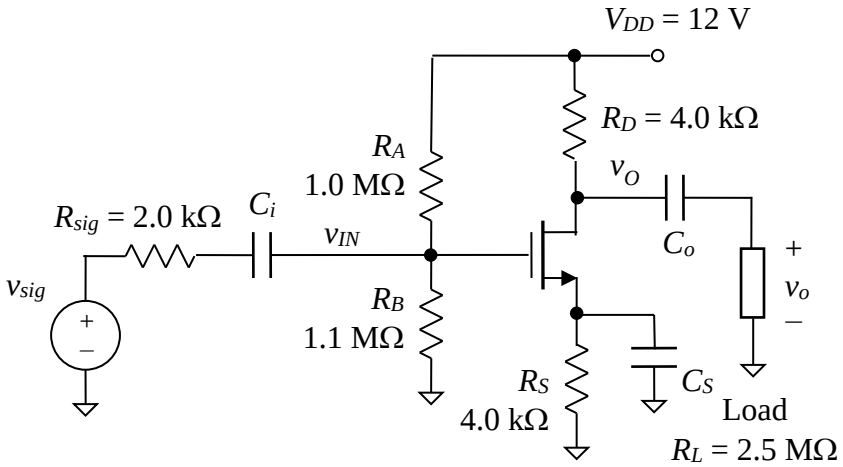
G Prob. 1 (continued): A smaller I_D leads to a smaller V_{OV}, which in turn leads to a tighter restriction on the magnitude of v_{gs}, which in the CS amplifier below is equal to the small-signal voltage v_{in}.

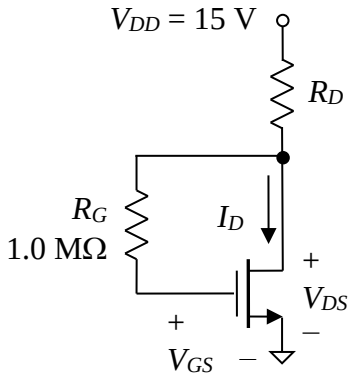
The designers of the amplifier decide to increase the gain by increasing the voltage across R_D to $0.4V_{DD}$ and decreasing the voltage across R_S to $0.26V_{DD}$ to compensate. They will also reduce I_D from 1.0 mA to 500 μA. Find:

- **a.** the new values of R_A, R_B, R_D, and R_S to meet the new specifications with the constraint that $R_A \| R_B \geq 500$ kΩ
- **b.** the new voltage gain $A_v = v_o/v_{in}$. Use a small-signal model for your analysis.
- **c.** the new limit on the input voltage magnitude $|v_{in}|$, assuming that a factor of 1/10 corresponds to "much less than"

The MOSFET's parameters are $k_n = 50$ mA/V^2 and $V_t = 2.0$ V. All of the capacitors have negligible reactances at the signal frequency.



2. The circuit shown at right is an alternative MOSFET bias network that uses a feedback resistor R_G between the gate and the drain terminals. It is used in situations when the source terminal must have a direct connection to ground. An analysis of the circuit to determine an expression for the quiescent drain current I_D is the focus of one of the ungraded problems below. The value of R_G is not usually critical in this type of circuit, but there are good reasons to make it a large value, so assume that $R_G = 1.0$ MΩ. If $k_n = 200$ mA/V^2 and $V_t = 2.0$ V for the MOSFET, find the value of R_D required to set the quiescent drain current to 500 μA. Also find the resulting quiescent value of V_{DS}.



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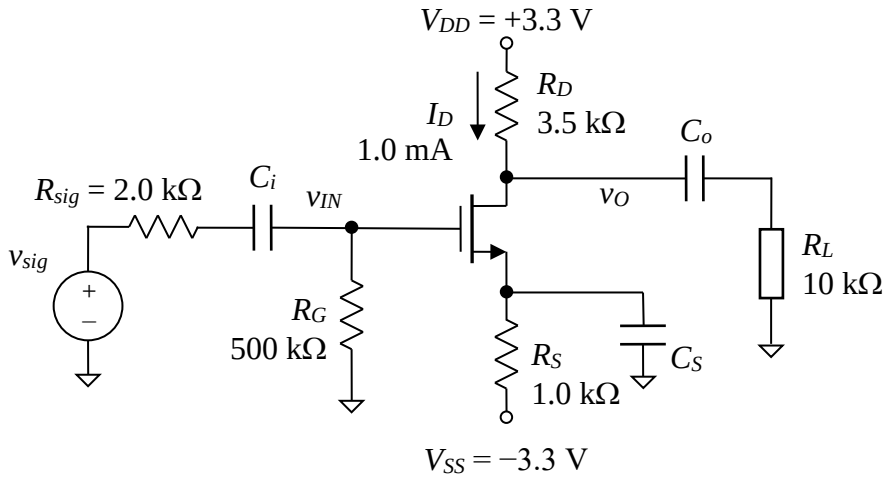
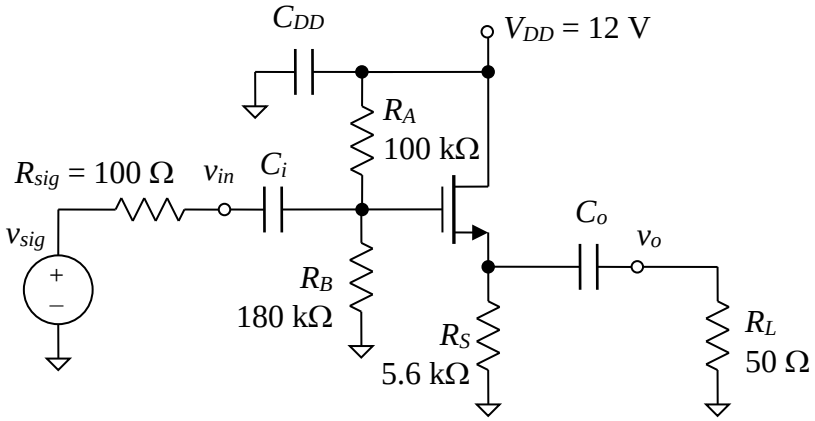
3. The *n*-channel MOSFET in the circuit shown below has $k_n = 800\ \mu A/V^2$ and $V_t = 0.70$ V. The circuit uses a bipolar (±3.3 V) power supply. The resistor values have been chosen to produce a quiescent drain current I_D of 1.0 mA and a quiescent value for V_{DS} that is 0.50 V above the triode-saturation boundary (defined by $V_{DS} = V_{GS} - V_t$). Assuming that $\lambda = 0$ (i.e., that there is no channel-length modulation), find the small-signal voltage gain v_o/v_{in} of the amplifier. Use a small-signal model for your analysis. You may assume that all three capacitors have negligible reactances over the operating frequency range of the amplifier.



4. Using small-signal analysis, find the small-signal voltage gain v_o/v_{in} of the source follower depicted below. The MOSFET has the parameter values $k_n = 200\ mA/V^2$ and $V_t = 2.0$ V You may assume that the MOSFET's small-signal output resistance $r_o \rightarrow \infty$ and that all three capacitors have negligible reactances at the operating frequency.



5. For any type of MOSFET amplifier circuit, the small-signal constraint is $|v_{gs}(t)| << 2V_{OV}$. That is, the magnitude of the signal component of v_{GS} at any point in time must satisfy the constraint. For the source follower circuit considered in the previous problem, find the corresponding constraint on the small-signal input voltage v_{in}. In other words, find the maximum value of $|v_{in}|$ so that v_{gs} does not violate the small-signal condition. Note that you must find a relationship between v_{in} and v_{gs} and then use the constraint on v_{gs} as a step toward finding one for v_{in}.

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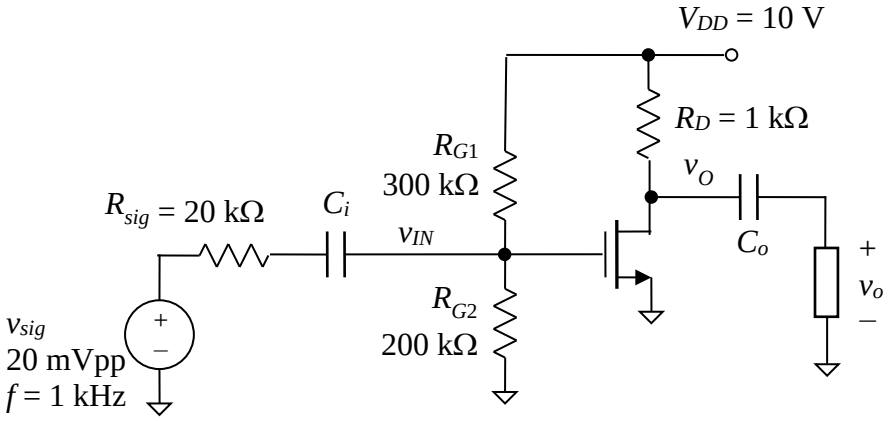
***Ungraded Problems*:**

The following problems will not be graded, but you should attempt to solve them on your own and then check the solutions. Do not give up too quickly if you struggle with one or more of them. Move on to a different problem and then come back to the difficult one after a few hours.

1. The common-source amplifier circuit shown below is not practical because there is no source degeneration resistor to stabilize the bias voltages and currents. However, some insights into amplifier operation can be gained from it. A sinusoidal signal $v_{sig}(t)$ with the indicated properties is applied to the input. (The phase doesn't matter, so assume that it is zero.) The MOSFET has the parameter values k_n = 1.0 mA/V^2 and V_t = 1.0 V. Since this is an amplifier, you may assume that the designers intended for the MOSFET to operate in the saturation region at all times. You may also assume that $\lambda = 0$, that all of the capacitors have negligible reactances at the signal frequency, and that the load acts like an open circuit.

- **a.** Use an appropriate small-signal model of the circuit to find the numerical value of the small-signal voltage gain $A_v = v_o/v_{in}$, assuming linear operation around the quiescent point.
- **b.** Suppose that the values of resistors R_{G1} and R_{G2} are changed so that the quiescent gate-to-source voltage V_{GS} is just barely above the threshold voltage V_t (i.e., the MOSFET is on the edge of the cut-off region). Find the value of the small-signal voltage gain A_v at the new operating point.
- **c.** Now suppose that the quiescent gate-to-source voltage V_{GS} has the value that causes the MOSFET to operate at the boundary between the saturation and triode regions, that is, at point B in Fig. 7.2b of Sedra & Smith, 7th ed. Find the small-signal voltage gain value for this case.

Note that in practice the amplifier should not be operated in either of the conditions represented by parts b and c because the output voltage has no room to swing above and below its quiescent value without the MOSFET entering the cut-off (part b) or triode (part c) region. The voltage gains found in the two parts represent theoretical lower and upper limits for this particular circuit.



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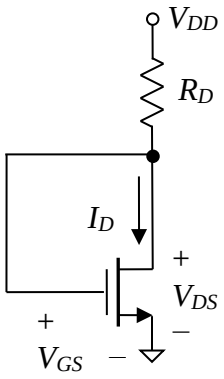
2. Measurements are performed on an *n*-channel MOSFET in a test configuration that has the gate shorted to the drain as shown at right. It is found that the DC drain current is 0.40 mA for $V_{GS} = V_{DS} = 1$ .0 V and 0.10 mA for $V_{GS} = V_{DS} = 0.80$ V. Use the measured data to estimate the values of k_n and V_t for the MOSFET. The tests assume that $\lambda = 0$ (i.e., there is no channel length modulation).



3. The circuit shown below right is an alternative MOSFET bias network that uses a feedback resistor R_G between the gate and the drain terminals. This technique can be used when stable bias is required but the source terminal must be grounded, as is sometimes the case in high-frequency circuits for which a source degeneration resistor in parallel with a bypass capacitor might not be able to provide a low-impedance path between the source and ground. That is, the parallel RC combination might have too much stray impedance at high frequencies. Show that the quiescent drain current is given by the expression for I_D below. *Hint*: Start the derivation with the KVL expression and its modifications shown above the expression for I_D. Note that $V_{DS} = V_{GS}$ because zero DC current flows through R_G.

$$V_{DD} = I_D R_D + V_{DS} = I_D R_D + V_{GS}$$

$$V_{DD} = \frac{1}{2} k_n R_D \left(V_{GS} - V_t\right)^2 + V_{GS}$$

$$V_{DD} - V_t = \frac{1}{2} k_n R_D \left(V_{GS} - V_t\right)^2 + V_{GS} - V_t$$

$$V_{DD} - V_t = \frac{1}{2} k_n R_D V_{OV}^2 + V_{OV}$$

$$I_D = \frac{1 + k_n R_D \left(V_{DD} - V_t\right) - \sqrt{1 + 2 k_n R_D \left(V_{DD} - V_t\right)}}{k_n R_D^2}$$