ECEG 350 **Electronics I** **Fall 2024**

Homework Assignment #6 – due via Moodle at 11:59 pm on Friday, Oct. 25, 2024

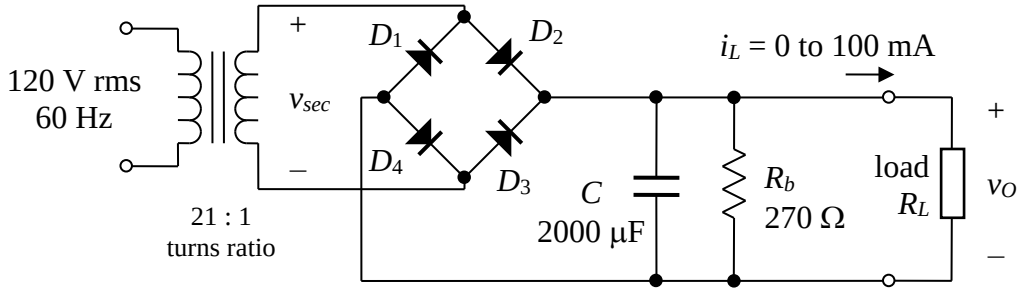
***Instructions, notes, and hints*:**

You may make reasonable assumptions and approximations to compensate for missing information, if any. Provide the details of all solutions, including important intermediate steps. You will not receive credit if you do not show your work.

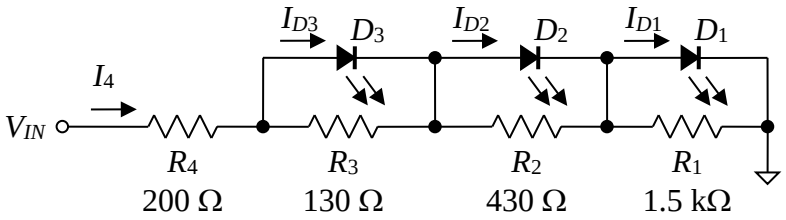
The first few problems will be graded and the rest will not be graded. Only the graded problems must be submitted by the deadline above. Do not submit the ungraded problems.

***Graded Problems*:**

1. The peak secondary winding voltage in the power supply circuit shown below is approximately 8.1 V. The rectifier diodes each have a turn-on voltage of 1 V and a maximum PIV (peak inverse voltage) or PRV (peak reverse voltage) rating of 100 V. The load draws a variable amount of current that can range from zero to 100 mA. Bleeder resistor R_b ensures that the filter capacitor discharges quickly when the power is shut off even if no load is present (i.e., if $R_L \rightarrow \infty$). A bleeder resistor is a safety feature included in most power supplies. Find the worst-case percentage ripple (relative to peak voltage) on the output voltage v_O for the component values shown. Also find the percentage of the AC waveform's period T during which any one of the rectifier's diodes conducts.



2. The circuit shown below is a simple bar graph display that uses red LEDs. It acts like a crude voltage level indicator. As voltage V_{IN} rises from zero, first D_1 turns on, then D_2 at a higher voltage, and finally D_3 at a still higher voltage. Find the value of V_{IN} at which diode D_2 just starts to turn on (and at which D_1 is also on). Also find the diode current I_{D1} at that value of V_{IN}. Assume that the constant-voltage model applies to the diodes with V_F = 2.0 V.



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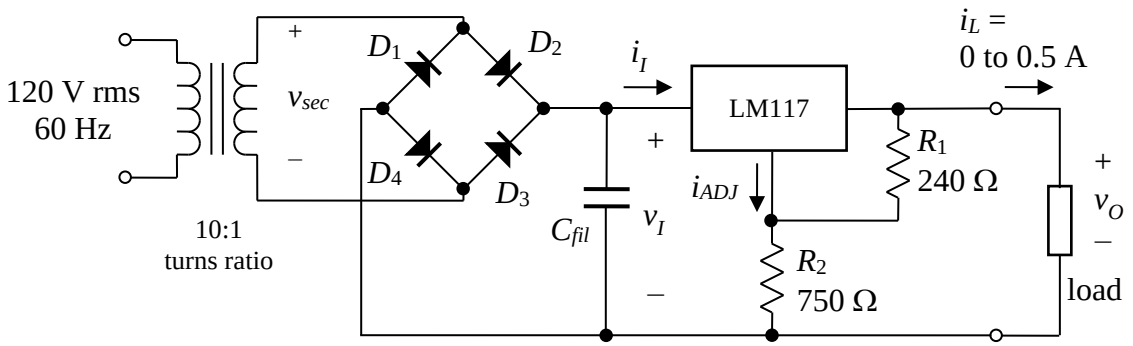
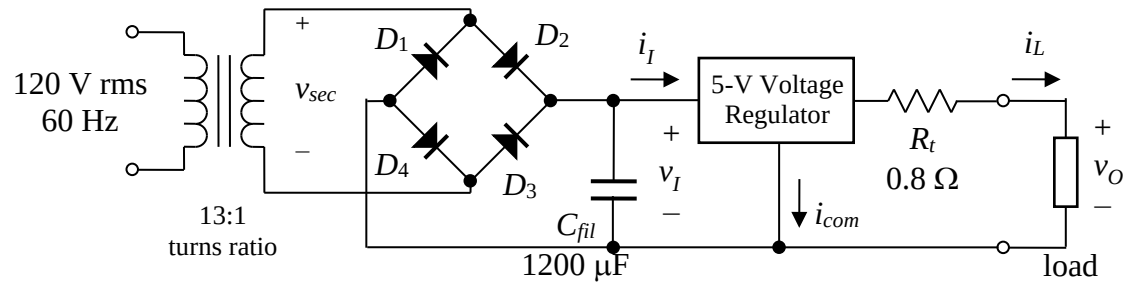
3. As shown below, an LM117 voltage regulator is used in a power supply circuit that includes a full-wave bridge rectifier and a filter capacitor C_{fil}. The rectifier diodes each have a turn-on voltage of V_F = 1.0 V, and the transformer's specified secondary winding voltage is 12 V rms. The values of resistors R_1 and R_2 have been set to produce a nominal output (load) voltage of v_O = 5.2 V. The largest expected load current is 500 mA. The drop-out voltage V_{DO} of the regulator is about 2 V. A datasheet for the LM117 and LM317 is available on the Laboratory page at the ECEG 350 course web site.

- **a.** By KCL, if the current i_{ADJ} in the common terminal of the regulator is negligible, then the input current i_I to the regulator circuit must be approximately the same as the load current i_L for large values of load current. About 5 mA flows through R_1 and R_2 at all times. Find the required value of capacitor C_{fil} so that the minimum voltage $V_{\min}$ across the capacitor is roughly 80% greater than $v_O + V_{DO}$.
- **b.** Find the worst-case ripple on the capacitor voltage for the case when the load draws a DC output current at the maximum value of 0.5 A. Assume that C_{fil} has the value found in part a.
- **c.** Use the information given in the datasheet to express the load regulation in mV/mA. Assume a typical case at 25 °C for the TO-220 package. Note that the data are given for an output current ranging from 10 mA to I_{MAX} = 1.5 A.



4. In the power supply circuit shown below, a three-terminal regulator provides a nominal voltage of 5 V to an amplifier module. Because of poor design technique, the circuit board trace between the output terminal of the regulator and the positive power supply terminal (the circle near the positive side of v_O) is too thin and has an equivalent resistance of 0.8 Ω. It is modeled as R_t in the diagram. The regulator itself has a specified load regulation of 0.008 mV/mA. Find the load regulation of the power supply circuit as a whole (i.e., including the effect of R_t). The rectifier diodes each have a turn-on voltage of 1.0 V, and the power supply is designed to provide up to 500 mA of current to the load. The current i_{com} (like i_{ADJ} in an adjustable regulator) is negligibly small.



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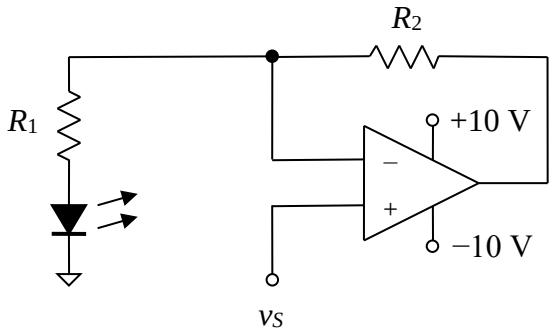
5. For the power supply circuit considered in the previous problem, find:

- **a.** the approximate ripple voltage across the filter capacitor C_{fil} at the maximum load current (500 mA).
- **b.** the approximate time-average power dissipated by the three-terminal regulator.
- **c.** the line regulation expressed in the %/V unit assuming that measurements reveal an output voltage ripple of 10 mV at the maximum load current of 500 mA.

6. The circuit shown below is designed to light the LED when voltage v_S ("S" subscript for "sense") is above the turn-on voltage of the LED, which is V_F = 1.8 V. The LED shines brighter as v_S rises. However, above a certain value of v_S the LED stops increasing in brightness as v_S continues to rise. Assuming that the constant-voltage model applies for the LED, find the standard 5% values of R_1 and R_2 that would cause the LED to reaches its maximum brightness at around v_S = 5.0 V and so that the maximum current through the LED is around 25 mA. The op-amp has the specifications given next to the figure. *Hint*: Aspects of the problem that do not have a significant impact on the determination of the resistor values can be ignored.



Op-Amp:
max. input offset voltage magnitude: 8.0 mV
max. input bias current: 100 nA
typ. open-loop voltage gain: 1.5×10^5
output voltage limits: ±9.0 V
output current limit: 35 mA

***Ungraded Problems*:**

The following problems will not be graded, but you should attempt to solve them on your own and then check the solutions. Do not give up too quickly if you struggle with one or more of them. Move on to a different problem and then come back to the difficult one after a few hours.

1. The power supply circuit shown on the next page is typical of those used to drive high-voltage circuits. Note that it uses a step-up transformer. Also note that the output voltage v_O is the sum of the two capacitor voltages. The load has a minimum equivalent resistance of 400 Ω, but it could be higher. ($R_{L\text{min}}$ is associated with the maximum possible load current. Smaller load currents correspond to larger equivalent load resistances.)

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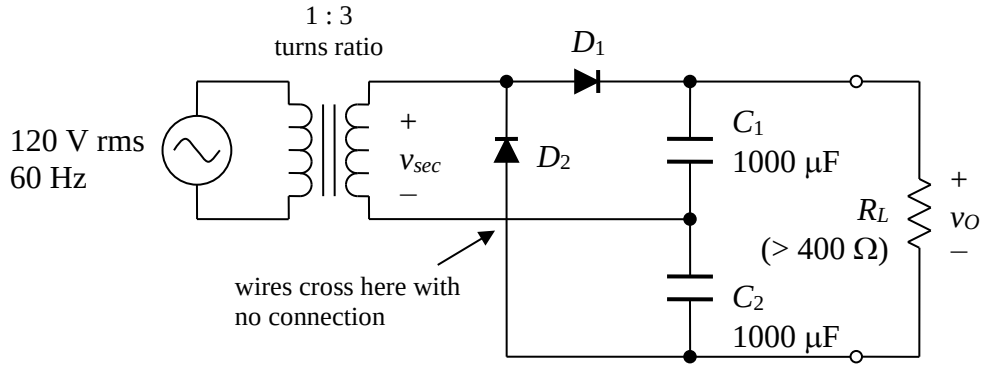
Complete the following analysis steps:

- **a.** Find the peak value of the secondary voltage v_{sec} of the transformer.
- **b.** Find the peak voltages across capacitors C_1 and C_2 if D_1 and D_2 are silicon diodes with turn-on voltages that are negligible compared to the secondary voltage.
- **c.** Find the approximate nominal output voltage v_O if the ripple voltage is negligibly small. *Hint*: This circuit called a *voltage doubler*, but you must show/explain why.
- **d.** Find the worst-case ripple voltage at the output (across the load R_L). The diodes conduct for only a tiny fraction of each period of the secondary voltage.
- **e.** Find the peak reverse-bias voltage experienced by each diode, assuming in this case that the voltages across C_1 and C_2 have negligible ripple.



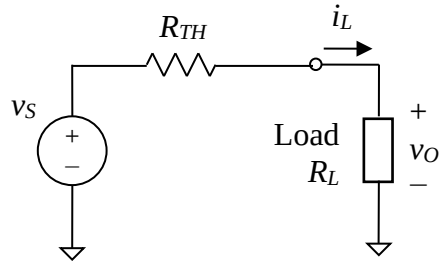
2. Convert the line regulation specification 0.05%/V to the mV/V unit for the case when the nominal output voltage of a regulator is 12 V and the maximum load current is 500 mA.

3. The datasheet for the LM78XX family of voltage regulators specifies that the typical load regulation is 9.0 mV under the condition that the output current varies from 5 mA to 1.5 A. Express the load regulation of the regulator in the mV/mA unit.

4. The datasheet for the LM78XX family of voltage regulators also specifies that the typical load regulation is 4.0 mV under the condition that the output current varies from 250 mA to 750 mA. Express the load regulation of the regulator in the mV/mA unit for this second specification.

5. Show that the expression for dv_O/di_L for any TEC like the one shown below right is equal to the negative of the Thévenin equivalent resistance; that is, prove the expression shown below left. Note that dv_O/di_L is equal to the load regulation for a voltage regulator circuit if the minus sign is ignored. Also note that $dv_O/di_L = \Delta v_O/\Delta i_L$ for the case of a purely resistive (real-valued) load and a purely resistive Thévenin equivalent impedance.

$$\frac{dv_O}{di_L} = -R_{TH}$$



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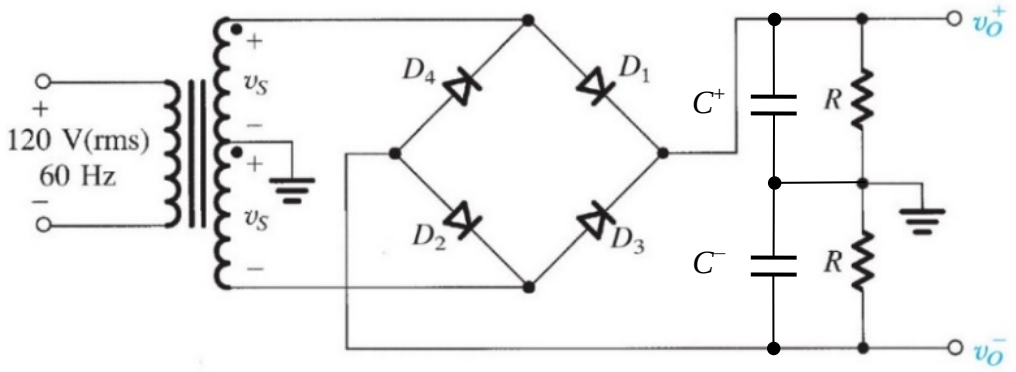
6. Consider the bipolar power supply circuit shown below (adapted from Fig. P4.74 of Sedra & Smith, 8th ed.). The circuit is not a full-wave *bridge* rectifier. It is actually two full-wave rectifiers with center taps that supply a positive voltage at node v_O^+ and a negative voltage at node v_O^- (both relative to ground). The dots next to the secondary winding are called phasing dots, and they indicate which ends of the respective windings are in phase. In the diagram, the upper end of the upper half of the secondary winding is positive at the same time as the upper (grounded) end of the lower half. The two secondary voltages labeled v_S are sinusoidal, equal to each other, and in phase. Two filter capacitors C^+ and C^- are to be connected across the loads R as shown to smooth the output voltage waveforms.

Find the required minimum value of the two capacitors for a maximum anticipated load current of approximately 1.0 A with a maximum ripple of 3% on each output voltage. Note that this is not a standard power supply design. You need to trace the current flow through the circuit during each half of the AC cycle. You might also need to modify any formula(s) that you use. You cannot assume that the positive and negative load currents (flowing through the upper or lower R) are exactly the same at any particular instant in time, but the currents are the same in a time-average sense because voltages v_O^+ and v_O^- on average are the same. The total secondary voltage is 18.4 V rms, so v_S = 9.2 V rms. The turn-on voltage of each diode is 1.0 V.



7. The circuit shown on the next page can be used to detect the presence of strong radio signals. An antenna, represented by the TEC consisting of voltage source $v_A(t)$ and resistance R_A, picks up the signal and produces a small AC voltage across its terminals *a*-*b*. The resulting current is rectified by the diode and filtered by the capacitor. This creates a DC current i_M (with ripple) that causes the needle in the old-fashioned d'Arsonval meter M to deflect. (See https://www.engineersedge.com/instrumentation/electrical_meters_measurement/darsonval_movement.htm.) Suppose that the meter is used to monitor the WKOK broadcast station near Sunbury, PA, which operates at a frequency of f = 1.070 MHz. A signal with peak value V_m is induced in the antenna as shown in the diagram. The meter gives a full-scale reading (maximum deflection of the indicator needle) for a current of 100 μA, and it has an equivalent resistance of 25 kΩ. Find the minimum capacitor value C required to keep the ripple on v_C below 10% during a full-scale reading. Also find the peak antenna voltage V_m that corresponds to a full-scale reading of 100 μA. The diode is a germanium type with a turn-on voltage V_F of 0.3 V. Assume that the constant-voltage diode model applies and that the Thévenin equivalent resistance R_A of the antenna is small enough to be ignored.

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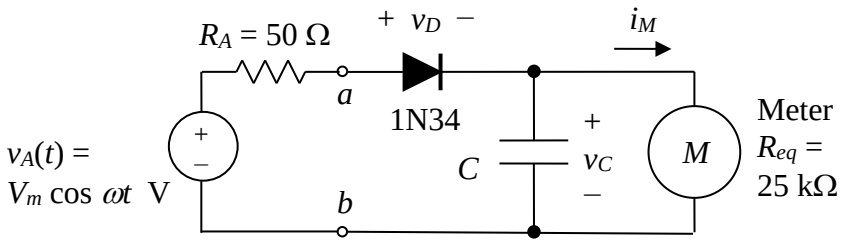

Circuit for Ungraded Problem 7.

8. In the previous problem, the antenna resistance R_A was ignored, and it was implicitly assumed that the capacitor voltage v_C follows the antenna voltage v_A. That is, the capacitor is assumed to charge to the voltage v_A instantaneously. That is not actually true. The voltage v_C lags the antenna voltage v_A slightly, and the delay depends on a time constant. As in the previous problem, the time constant is often assumed to be so short relative to the AC waveform's variations that it can be neglected. Using the value of capacitor C found in the previous problem, find the time constant that governs the charging of the capacitor, and show that it is in fact significantly smaller than the period of the AC waveform. *Hint*: You will need to find the TEC of the circuitry "seen" by the capacitor when the diode is on. That TEC is *not* the same as the v_A-R_A one (although it might be close). The circuit elements v_A and R_A comprise the TEC of only the antenna.