ECEG 350 Electronics I Fall 2024

Homework Assignment #2 – due via Moodle at 11:59 pm on Friday, Sept. 13, 2024
[Graded Probs. 4 and 5 revised 9/12/24]

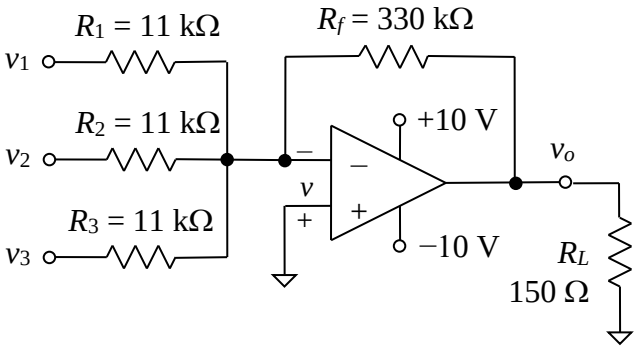
***Instructions, notes, and hints*:**

You may make reasonable assumptions and approximations in order to compensate for missing information, if any. Provide the details of all solutions, including important intermediate steps. You will not receive credit if you do not show your work.

Note that the first few problems will be graded and the rest will not be graded. Only the graded problems must be submitted by the deadline above. Do not submit the ungraded problems.

Graded Problems:

1. An LM741C op-amp is used in the summing amplifier shown below. The output voltage v_o can swing to ±8.5 V. The output is connected to a recording device that has an input resistance of 150 Ω, which acts like a 150 Ω load on the summing amp. Input terminals v_1 through v_3 are connected to pressure sensors that can be modeled as ideal voltage sources. The first two sensors are exposed to constant pressures and produce DC output voltages of v_1 = 15 mV and v_2 = 24 mV. The third sensor is exposed to an exponentially increasing voltage that starts at $v_3(0)$ = 0 V and approaches 120 mV after a long period of time according to the expression for v_3 given below. Find the moment in time at which the op-amp experiences output current limiting, and find the corresponding output voltage v_o. Also find the value of the voltage v across the op-amp's input terminals after v_3 has stabilized at its final voltage. You will need to consult the LM741C op-amp datasheet (available on the Laboratory page at the course web site) to obtain the typical value of the output current limit.



$$v_3(t) = 0.120\left(1 - e^{-0.125t}\right) \text{ V, t > 0.}$$

2. Now suppose that the recording device connected to the output of the summing amplifier in the previous problem is replaced with a new one with an equivalent input resistance of 800 kΩ, which is so high that output current limiting is no longer a concern. However, the output voltage of the sensor connected to terminal v_1 rises to 450 mV due to a significant increase in the measured pressure. Determine whether the op-amp experiences output voltage clipping after voltage v_3 reaches its maximum value and, if so, find the value of voltage v between the input terminals. The other circuit quantities and op-amp properties are the same as in the previous problem.

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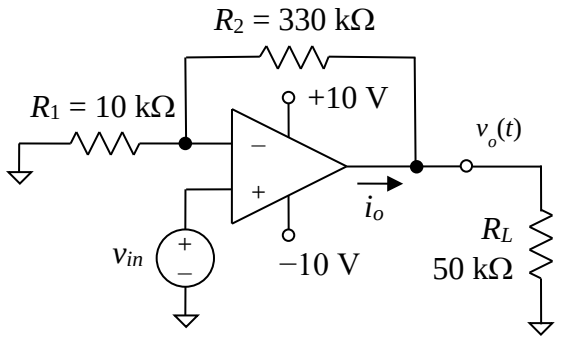
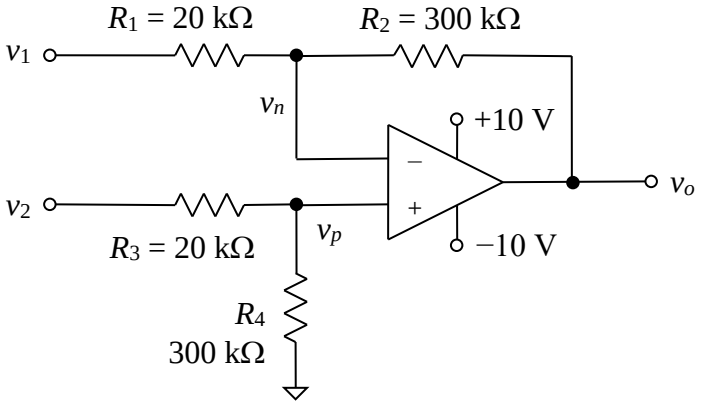
3. The input signal v_{in} supplied to the amplifier circuit shown below is an AC voltage that can be expressed as $v_{in}(t) = V_m \cos(32{,}000\pi t - 60°)$ V, where V_m is the amplitude of the voltage. Find the maximum value that V_m can have to avoid clipping of the output voltage v_o. Assume that the actual output voltage limits are +8.5 V and −8.0 V. You may ignore the effects of the input offset voltage and input bias currents since they will be negligible in this case.



4. **[text in boldface revised 9/12/24]** In the diff amp circuit shown below, the single-ended input voltages are v_1 = 680 mV and v_2 = **1,240** mV. Assuming that the op-amp is ideal and that the resistors have the exact values shown, find the output voltage v_o using the two methods listed below. Also find the node voltages v_n.and v_p.

- **a.** Find the differential-mode input voltage v_{Id}, and then use the differential-mode gain to find the output voltage.
- **b.** Use superposition to find the output voltage by activating v_1 and v_2 one at a time and then adding their effects. Note that because you are applying the superposition method, you may ignore any output voltage clipping that might result when only one source is activated.



5. **[text in boldface revised 9/12/24]** Find the output voltage for the diff amp in the previous problem if the single-ended input voltages are v_1 = 680 mV and v_2 = **−240** mV. Find the node voltages v_n.and v_p as well. Be careful! Continue to assume that the op-amp is ideal and that the resistors have the exact values shown.

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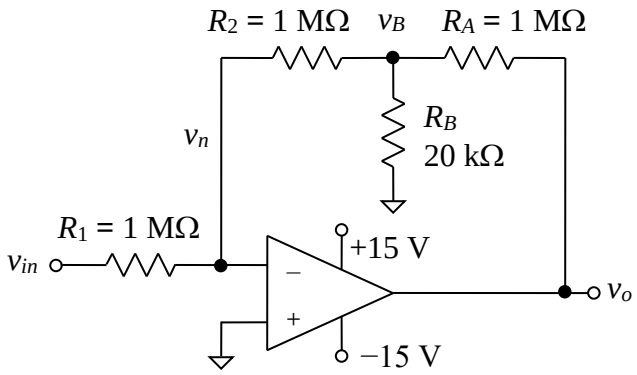
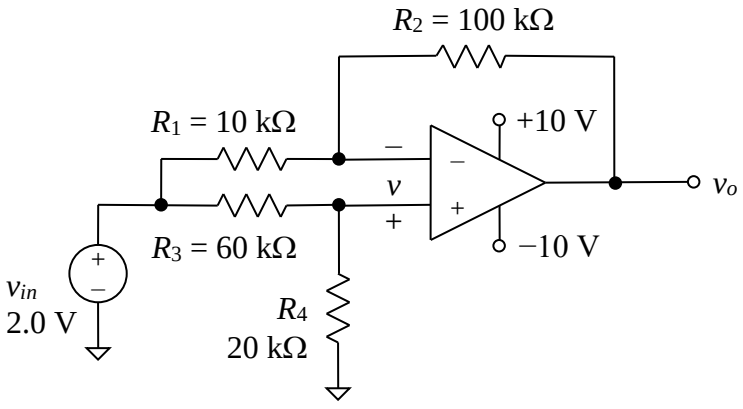
***Ungraded Problems*:**

The following problems will not be graded. They are intended to serve as practice problems and examples. The solutions will be posted along with the solutions to the graded problems. You should attempt to solve them on your own and then check the solutions afterwards. Do not give up too quickly if you struggle with any of them. Move on to a different problem and then come back to the difficult one after a few hours.

1. For the amplifier shown below, assume that the input bias currents of the op-amp are unknown but that $I_{B1} \approx I_{B2}$. To mitigate the effect of the input bias currents on the output voltage, a resistor R_x will be inserted in series with the noninverting input terminal of the op-amp. Find the required value of resistor R_x.



2. Show that the op-amp in the circuit diagram below saturates at one of the power supply voltages, and find the resulting voltages v and v_o. Note that the circuit is not a diff amp because $R_4/R_3 \neq R_2/R_1$, not even approximately. You may ignore the minor effects of the input offset voltage and input bias currents of the op-amp. Assume that v_o can swing all the way from −10 V to +10 V.



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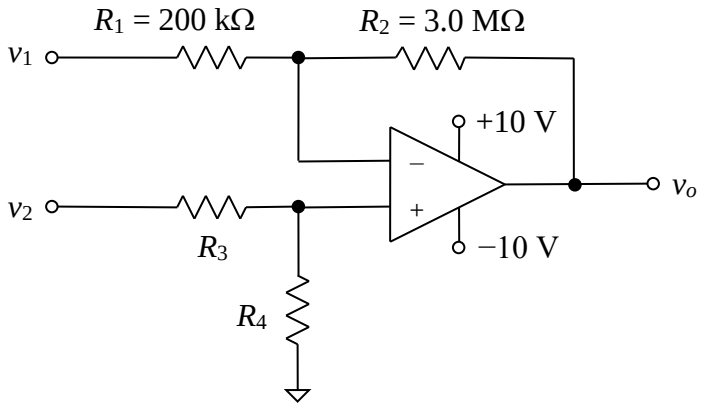
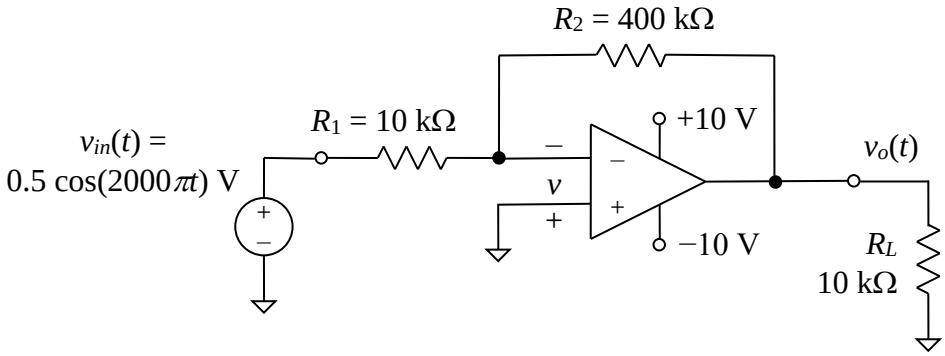
3. In the circuit shown below, the op-amp has input bias currents of roughly 80 nA flowing into each terminal (i.e., $I_{B1} \approx I_{B2}$). Find the approximate output voltage v_o (to two digits of accuracy since the resistor values are given to only two digits) due only to the two input bias currents (i.e., for the case $v_1 = v_2 = V_{OS} = 0$) for the following two sets of values for resistors R_3 and R_4, and explain the significance of the results. The resistor tolerances are 0.1%. Note that the differential-mode gain is the same (15 V/V) for both parts; although R_3 and R_4 in part **b** do not have the same nominal values as R_1 and R_2, their ratio is the same.

a. $R_3 = 200$ kΩ and $R_4 = 3.0$ MΩ (same as R_1 and R_2)
b. $R_3 = 10$ kΩ and $R_4 = 150$ kΩ (same ratio as R_2/R_1)



4. Sketch at least one cycle of the voltage v as a function of time for the circuit shown below. The amplifier goes into saturation (i.e., the output clips) during parts of the AC cycle. Find the first four instances in time after $t = 0$ when the amplifiers transitions from linear operation to clipping or vice versa. The load is another amplifier with an input resistance represented by the equivalent resistance R_L. (That is, the load resistance of the amplifier below is the same as the input resistance of the following amplifier.) You may ignore the input offset voltage and input bias currents of the op-amp.



5. For the amplifier circuit considered in the previous problem, assume that the magnitude of the input voltage v_{in} is reduced from 0.5 V to 0.1 V and that the load is replaced with a new one with an equivalent resistance R_L of 100 Ω. If the output current limit rating of the op-amp is 25 mA, sketch the output waveform for one complete AC cycle. You may ignore the input offset voltage and input bias currents of the op-amp.

6. For the circuit considered in the previous problem (in which v_{in} has a magnitude of 0.1 V), find the voltage v at the instant when the input voltage v_{in} is at its peak positive value.