ECEG 350 Electronics I Fall 2024

Homework Assignment #1 – due via Moodle at 11:59 pm on Friday, Sept. 6, 2024

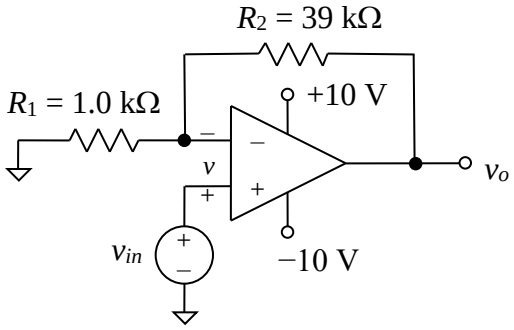
***Instructions, notes, and hints*:**

You may make reasonable assumptions and approximations in order to compensate for missing information, if any. Provide the details of all solutions, including important intermediate steps. You will not receive credit if you do not show your work.

Note that the first few problems will be graded and the rest will not be graded. Only the graded problems must be submitted by the deadline above. Do not submit the ungraded problems.

Graded Problems:

1. Shown below is a noninverting amplifier circuit. The small triangles represent connections to the reference or ground node. The small circles with "+10 V" and "−10 V" written next to them represent connections to DC power supplies. Remember that current can flow into and/or out of those terminals; they are not unconnected wire ends.



The closed-loop voltage gain v_o/v_{in} with the finite open-loop gain A_o accounted for is given by

$$A_v = \frac{v_o}{v_{in}} = \left(1 + \frac{R_2}{R_1}\right) \frac{1}{1 + \dfrac{1 + R_2/R_1}{A_o}} .$$

The expression reduces to the ideal formula $(1 + R_2/R_1)$ for the case when $A_o \to \infty$. For v_{in} = 25 mV DC, find numerical values to two digits of accuracy (i.e., using two significant digits) for the output voltage v_o and the voltage v between the op-amp's inputs for the following three values of the open-loop gain (the first two are unrealistically low):

a. $A_o = 50$
b. $A_o = 1{,}000$
c. $A_o \to \infty$

Briefly comment on the significance of your answers, and find the value of A_o for which the difference between the ideal gain and the actual gain is only 1%.

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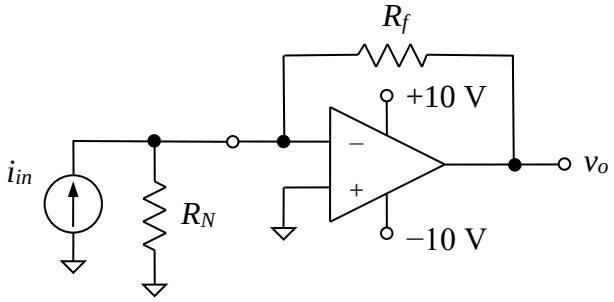
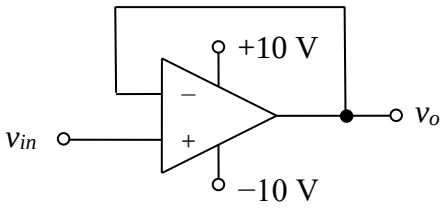
2. A circuit like the one shown below can be used to measure small currents. The independent current source i_{in} and resistor R_N on the left of the diagram represent the Norton equivalent circuit (NEC) of a circuit or sensor under test that is not shown. (The small circle next to the NEC represents the input terminal of the op-amp circuit. It can be considered part of the conductor between the NEC and the inverting terminal of the op-amp.) If the op-amp were ideal (i.e., if $A_o \to \infty$), then the output voltage v_o would be related to the input current i_{in} via $v_o = -R_f\, i_{in}$. Find the relationship between v_o and i_{in} for the case when the op-amp has a finite open-loop gain A_o and the Norton equivalent resistance R_N is also finite. You may assume that there are no other non-ideal effects, such as input offset voltage or input bias currents, that affect operation. Try to apply algebraic manipulation to express the gain formula in such a way that the reduction to the simple form for $A_o \to \infty$ is obvious. Deriving more useful forms of expressions is a good skill to develop; it can provide an effective way to check your derivations. *Thought question (not graded)*: If A_o is large (say, 10^5 or greater), how small can R_N be relative to R_f so that the approximation $v_o \approx -R_f\, i_{in}$ is still a good one?



3. Find an expression for the voltage gain v_o/v_{in} for the voltage follower circuit shown below that accounts for the finite open-loop voltage gain A_o of the op-amp. You may assume that there are no other non-ideal effects present in the circuit. Note that $v_o/v_{in} = 1$ in the ideal case. The small circle with "v_{in}" written next to it represents the single-ended input terminals of the amplifier circuit. An unknown external circuit or sensor would be connected there. Thus, you should assume that current can flow into and/or out of that terminal (if, in fact, current can flow into or out of the op-amp's noninverting terminal; can it?) and that it has the voltage v_{in} between it and ground. If you wish, you may add an independent voltage source v_{in} between that node and ground for your derivation. Although the ground node is not explicitly indicated in the circuit, the voltages v_{in}, v_o, +10 V, and −10 V are all defined with respect to the ground node. It is common practice to omit voltage sources that represent DC power supplies and independent signal voltages in this way to reduce the visual clutter in circuit diagrams. The small circle with "v_o" written next to it represents the single-ended output terminals (i.e., voltage v_o is measured from the circle to ground.)



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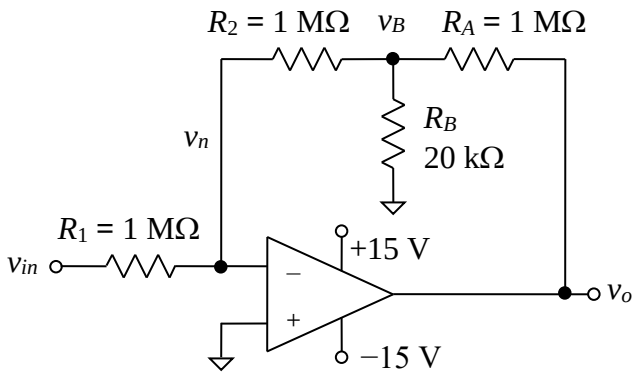
4. The amplifier shown below uses an unusual feedback network to achieve a high closed-loop voltage gain of −52 V/V with modest resistor values (a few megohms or less) while also allowing the value of R_1 to be high. The latter feature is important because R_1 sets the input resistance of the amplifier; high input resistance is desirable in voltage amplifiers. Suppose that the input offset voltage V_{OS} of the op-amp is 3.0 mV. Find the output voltage due to the input offset voltage when the input signal (the voltage v_{in} applied to the input terminal at the left-hand end of the circuit) is zero. Provide the answer for both possible polarities of the input offset voltage. You may ignore the effects of the finite open-loop gain and input bias currents of the op-amp; that is, except for the nonzero input offset voltage, the op-amp is ideal. Note that setting $v_{in} = 0$ is equivalent to grounding the input terminal. Voltages v_{in}, v_o, v_n and v_B are all node voltages.



5. The previous problem illustrates that amplifiers with T-shaped feedback networks exacerbate the effect of the input offset voltage V_{OS}. They do the same thing with one of the input bias currents. Suppose that the op-amp in the previous problem has $I_{B1} = 75$ nA (into the inverting terminal) and $I_{B2} = 85$ nA (into the noninverting terminal). Find the output voltages due to I_{B1} and I_{B2} alone when the input signal voltage is zero (i.e., $v_{in} = 0$). Also ignore the effects of the finite open-loop gain and the input offset voltage.

***Ungraded Problems*:**

The following problems will not be graded. They are intended to serve as practice problems and examples. The solutions will be posted soon. You should attempt to solve them on your own and then check the solutions afterwards. Do not give up too quickly if you struggle with any of them. Move on to a different problem and then come back to the difficult one after a few hours.

1. Shown at the top of the next page is a noninverting amplifier circuit. Assuming that the op-amp is ideal, find the range of possible values for the closed-loop gain v_o/v_{in} if both resistors have 5% tolerance (i.e., their actual values lie within ±5% of their nominal or labeled values). Comment on whether the assumption of infinite open-loop gain (i.e., the ideal op-amp assumption) or the potential resistor value variation leads to greater error in the determination of the voltage gain. That is, is the error due to nonideal resistor values likely to be greater or smaller than the error due to assuming that the open-loop gain is infinite? Recall that $A_o > 10^5$.

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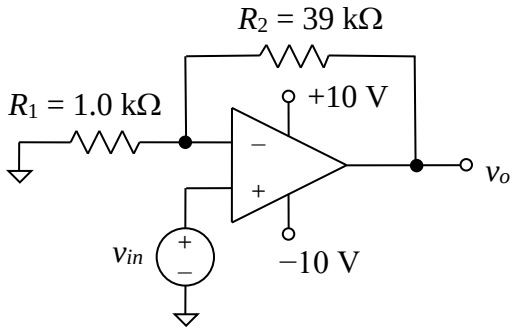
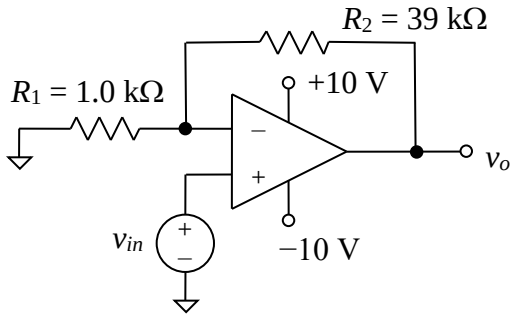
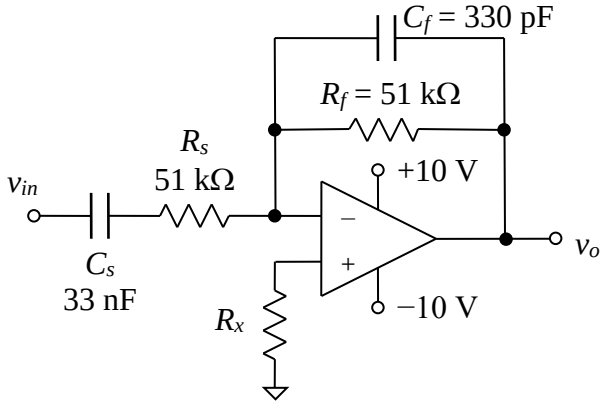


Circuit diagram for Ungraded Prob. 1

2. For the circuit shown below, find the value of a resistor R_3 that can be placed in series with the input voltage v_{in} to minimize the effects of the input bias currents I_{B1} and I_{B2}, assuming that $I_{B1} \approx I_{B2}$. Assume that the input offset voltage effect as negligible. If you think that you know the answer without circuit analysis, perform the analysis anyway for confirmation. Does the effect of R_3 depend on whether it is placed above or below v_{in} (assuming that v_{in} does not have to be grounded on the negative side for some reason)? Why or why not?



3. For the band-pass filter circuit shown below, find the value of R_x required to mitigate the effects of the input bias currents in the DC steady-state case, assuming that $I_{B1} \approx I_{B2}$. That is, find the value required to force $v_o = 0$ when $V_{OS} = v_{in} = 0$ but I_{B1} and I_{B2} are nonzero. Recall that DC steady state occurs after the transient period has ended. In the specific case of this circuit, steady state occurs after the capacitors have finished charging or discharging to their DC average values.



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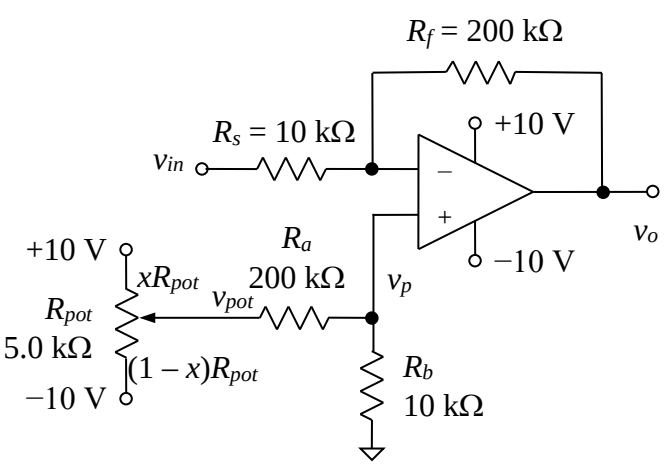
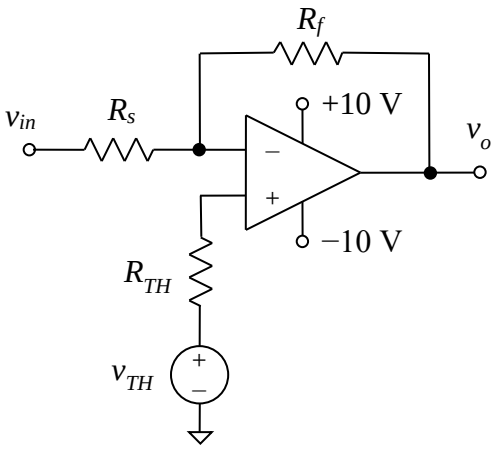
4. The circuit shown below left is an inverting amplifier intended for an application that requires the elimination of the combined input offset voltage and input bias current effects. For the particular op-amp used, it turns out that the values are V_{OS} = 3.5 mV, I_{B1} = 72 nA, and I_{B2} = 84 nA. Unfortunately, the op-amp does not have offset null terminals, so potentiometer R_{pot} and some fixed resistors will be used to "tune out" the output voltage error. The upper part of the potentiometer (between the potentiometer's wiper terminal, indicated by the arrow, and the +10 V supply) has a value of xR_{pot}, where $0 < x < 1$. The lower part has a value equal to the remaining resistance, which is $(1 - x)R_{pot}$. The value of x changes as the wiper is moved; that is, the wiper acts as a "tap" along the resistor. The potentiometer does not technically act like a simple voltage divider here because the combined resistance of R_a and R_b loads it down; however, the value of R_a is so large that its loading effect can be considered negligible (200 kΩ >> 5 kΩ). Because R_a is much larger than R_b, the voltage v_p at the op-amp's noninverting terminal is considerably smaller than the value of node voltage v_{pot}. Find the required setting for the potentiometer (i.e., find the value of x) to zero the output voltage v_o for the values of V_{OS}, I_{B1}, and I_{B2} given above when v_{in} = 0. It might help to note that the combination of the potentiometer, R_a, and R_b can be represented by a Thévenin equivalent circuit as shown in the diagram below right.



Original Circuit



Equivalent Circuit