Computer Architecture

Instructor

Assistant Professor Alan Marchiori

- **Office**: Breakiron 268
- **Office Hours**: By appointment; **Schedule an appointment**
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License

Course Description

Use a hardware description language to describe and design digital systems. Processor design, pipelining, cache and storage systems. Instruction and thread level parallelism, speculation, branch prediction.

Course Objectives

By the end of the semester, students are expected to be able to:

- Design, simulate, and describe the complete operation of a computer system (ABET a, b, c, k).
- Understand and apply computer architecture principles such as Amdahl's law, parallelism and locality to analyze the performance of different computer systems. (ABET a, e).
- Identify and utilize the various forms of parallelism (ILP, DLP, TLP, etc) to increase system performance.

ABET Outcomes

a. An ability to apply knowledge of mathematics, science, and engineering
b. An ability to design and conduct experiments, as well as to analyze and interpret data
c. An ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability
d. An ability to function on multidisciplinary teams
e. An ability to identify, formulate, and solve engineering problems
f. An understanding of professional and ethical responsibility
g. An ability to communicate effectively
h. The broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context
i. A recognition of the need for, and an ability to engage in life-long learning

j. A knowledge of contemporary issues
k. An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.

Textbook

Recommended

- Hennessy and Patterson, "Computer Architecture: A Quantitative Approach", 5th Edition. ISBN 978-0123838728. One copy is on reserve fro this course at the library. The library also has the eBook version available (Bucknell login required).
- Patterson and Hennessy, "Computer Organization and Design: The Hardware/Software Interface", 5th Edition. ISBN 978-0124077263. This is the required text for CSCI206. One copy is on reserve for this course at the library. The eBook is not yet available.

Reference

- Samir Palnitkar, "Verilog HDL", 2nd Edition. ISBN 978-0132599702. One copy is on reserve for this course at the library. No eBook.

Lecture

- CSCI320-01 -- MWF @ 2:00pm - 2:52pm in Dana Engineering 137

Lab

Section	Days	Time	Location
CSCI320L-61	T	8:00am - 9:52am	Breakiron Engineering 164
CSCI320L-60	T	10:00am - 11:52am	Breakiron Engineering 164

Policies

Attendance and Participation

An important part of the class is your active participation in lecture sections. If people do not show up to lecture, or do other work (or sleep) while in lecture, it degrades the quality of the class for everyone. Therefore, all students are expected to attend and actively participate in all lectures. If you have to miss a class please contact the instructor **at least 24 hours prior to the start of that class**. You will be responsible for making up any/all missed work.

Grading

Your instructor will make every effort to promptly return all graded work to you (usually by the next schedule class). Overall grades will be sent to you via your Bucknell email address after the first midterm exam and again in the last week of classes. If you would like to discuss your grade at any

time, please make an **appointment**.

Component	Grade
Course Project (Lab)*	50%
Activities & Quizzes	10%
Midterm Exam	15%
Final Exam*	25%

***** to pass the course you must pass both the Verilog Project and Final exam (separately).

Letter grades will then be assigned using the typical scale:

Score	Grade
93	A
90-92	A-
87-89	B+
83-86	B
80-82	B-
77-79	C+
73-76	C
70-72	C-
60-69	D
<60	F

Bonus points may occasionally be available.

If you think you find a grading error, you may request a regrade. Regrade requests must be recieved no later than **72 hours after the assignment/exam is returned**. It is possible for the new grade to be lower than the original grade. In all cases the most recent grade is used (not the highest grade).

Late Work

Late work will not be accepted unless you receive permission from the instructor **>24 hours before it is due**.

Accommodations

If you have a University recognized accommodation please let your instructor know. Your instructor will be happy to work with you.

Bucknell University Honor Code

As a student and citizen of the Bucknell University community:

1. I will not lie, cheat, or steal in my academic endeavors.

2. I will forthrightly oppose each and every instance of academic dishonesty.
3. I will let my conscience guide my decision to communicate directly with any person or persons I believe to have been dishonest in academic work.
4. I will let my conscience guide my decision on reporting breaches of academic integrity to the appropriate faculty or deans.